كتاب تجارب معمل

الاتصالات الرقمية

أولا: بيانات المعمل الأساسية

- **اسم المعمل**: معمل الاتصالات الرقمية
- **القسم العلمي**: قسم هندسة الالكترونيات والاتصالات
- **المشرف**: ا.د/ فايز ونيس
- **مهندس المعمل:** م/ نرمين عبد اللطيف أحمد
- **أمين المعمل**: أ/ وسام السيد
- **تليفون:** 1295
- **الموقع:** الدور الثالث، المعامل البحرية أمام صالات عمارة
- **مساحة:** 127 متر^2

ثانيا: قائمة بالأجهزة والمعدات الموجودة بالمعمل:

Serial number	العدد	الجهاز
1299	2	جهاز آفوميتر رقمي
3055	2	جهاز قياس التردد frequency counter
3400	1	مولد ذبذبات
3200	4	Digital multimeter
1399	1	Power supply
3200	1	storage oscilloscope Pm 33351401
1102	1	جهاز اوسيلسكوب محمول
1102	1	Digital storage oscilloscope 6DS 1102
-	1	بوصه Dig lc شاشه
-	1	جهاز كمبيوتر بدون شاشه
6000	1	Digital communication system treaner model 6000
1200	1	50 MHZ Digital storage oscilloscope
-	2	Electrical communication course comprising
-	1	Analog communication system
6000	1	Digital communication spec_ come 6000
2003	4	Multiple signal and power supply model Nsa2003
530	1	Micro wave trainer feedback model MW530
343	2	Opentenel OAT 343
6200	3	Power supply model 62002

ثالثا: قائمه بالتجارب التى تؤدي داخل المعمل:

م	التجربة	الغرض منها
1	Pulse code modulation	Convert the electronic signal from analog to digital
2	Amplitude shift keying modulator	control the signal amplitude to send it from transmitter to receiver in a correct shape
3	Amplitude shift keying demodulator	get the original signal back
4	frequency shift keying modulator	control the signal frequency to send it from transmitter to receiver in a correct shape
5	frequency shift keying demodulator	get the original signal back
6	phase shift keying modulator	control the signal phase to send it from transmitter to receiver in a correct shape
7	phase shift keying demodulator	get the original signal back
8	Line code encoder and decoder	Encoding the electronic transmitted signal and encoding the electronic received signal

رابعا الخدمات المجتمعية التي يؤديها المعمل:

1. **عدد المستفيدين من المعمل**: طلاب قسم هندسه الاتصالات والالكترونيات (4 دفعات)، طلاب قسم حاسبات (4 دفعات)، طلاب قسم كهرباء (4 دفعات)، طلاب قسم ميكانيكا (4 دفعات)، طلاب قسم برنامج الهندسة الطبية (4 دفعات)، طلاب قسم برنامج الهندسة الاتصالات (4 دفعات)، طلاب قسم برنامج ميكاترونيكس (4 دفعات)، طلاب الدراسات العليا
2. **الجهات التي تتعامل مع المعمل:** قسم هندسه الاتصالات والالكترونيات، شركات التدريب (كورسات PCB),مدارس الثانوي الفني
3. **الدخل السنوي: لا يوجد.**

4.الجهات الممولة لأنشطه المعمل: قسم هندسه الاتصالات والإلكترونيات والبرامج الخاصة

5. المشاريع التنافسية التي يشارك فيها المعمل:مشاريع تخرج لطلاب قسم هندسه الاتصالات والالكترونيات دفعة سنه رابعة، مسابقات مجمعه لطلاب قسم الانصالات وقسم حاسبات وقسم كهربا وقسم ميكانيكا

Unmanned Ground Vehicle Competition

خامسا الخدمات الطلابية:

1. **عدد المستفيدين من المعمل**: طلاب قسم هندسه الاتصالات والالكترونيات (4 دفعات)، طلاب قسم حاسبات (4 دفعات)، طلاب قسم كهرباء (4 دفعات)، طلاب قسم ميكانيكا (4 دفعات)، طلاب قسم برنامج الهندسة الطبية (4 دفعات)، طلاب قسم برنامج الهندسة الاتصالات (4 دفعات)، طلاب قسم برنامج ميكاترونيكس (4 دفعات)، طلاب الدراسات العليا
2. **الأقسام العلمية المستفيدة من المعمل:** قسم هندسه الاتصالات والالكترونيات (4 دفعات)، قسم حاسبات (4 دفعات)، قسم كهرباء (4 دفعات)، قسم ميكانيكا (4 دفعات)، قسم برنامج الهندسة الطبية (4 دفعات)، قسم برنامج الهندسة الاتصالات (4 دفعات)، قسم برنامج ميكاترونيكس (4 دفعات)
3. **الفرق الدراسية التي تستخدم المعمل:** طلاب قسم هندسه الاتصالات والالكترونيات (4 دفعات)، طلاب قسم حاسبات (4 دفعات)، طلاب قسم كهرباء (4 دفعات)، طلاب قسم ميكانيكا (4 دفعات)
4. **المقررات التي يتم تدرسها في المعمل:** سكاشن شرح للأجهزة القياس والعرض الإلكترونية وكيفية استخدمها وصيانتها وسكاشن شرح لتجارب اتصالات خاصة بالدفعة الرابعة في قسم الاتصالات والالكترونيات
5. **الرسائل العلمية:** رسائل علميه خاصة بهندسة الاتصالات والالكترونيات
6. **الدورات:** دورات تدربيه خاصة بصيانة الأجهزة القياس والعرض الإلكترونية ودورات برمجه للدوائر الإلكترونية
7. **الدراسات العليا:** يوجد محاضرات خاصة بتدريس مواد تمهيدي ماجستير بقسم هندسه الاتصالات والالكترونيات
8. **المسابقات:** مسابقات خاصة تصميم روبوتات وبرمجه للدوائر الإلكترونية
9. **الأنشطة:** مشاريع تخرج خاصة بطلاب هندسة الاتصالات والالكترونيات

Experiment 1

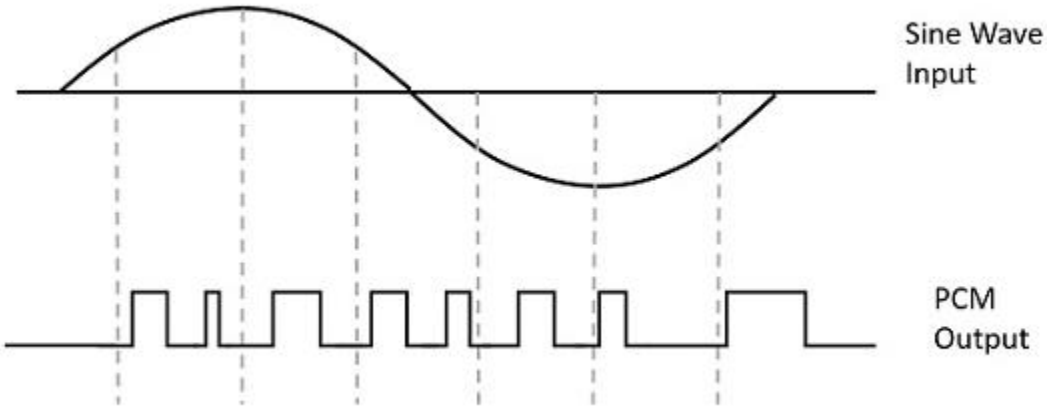
Pulse code modulation

Modulation is the process of varying one or more parameters of a carrier signal in accordance with the instantaneous values of the message signal.

The message signal is the signal which is being transmitted for communication and the carrier signal is a high frequency signal which has no data, but is used for long distance transmission.

There are many modulation techniques, which are classified according to the type of modulation employed. Of them all, the digital modulation technique used is **Pulse Code Modulation (PCM)**.

A signal is pulse code modulated to convert its analog information into a binary sequence, i.e., **1s** and **0s**. The output of a PCM will resemble a binary sequence. The following figure shows an example of PCM output with respect to instantaneous values of a given sine wave.



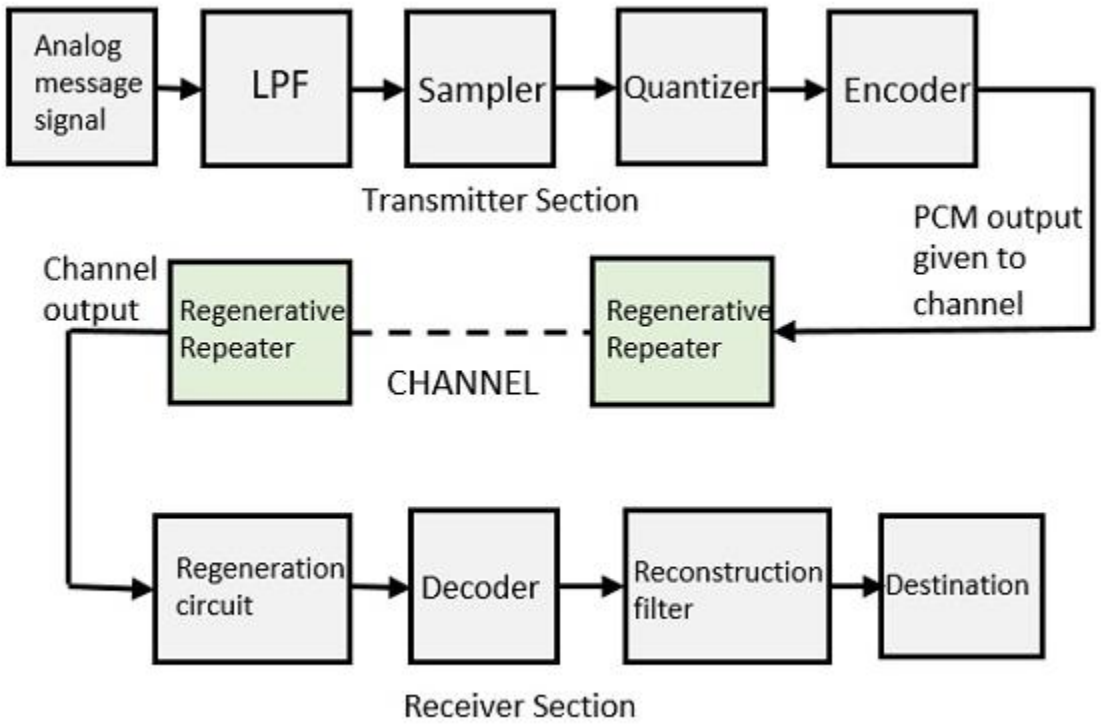
Instead of a pulse train, PCM produces a series of numbers or digits, and hence this process is called as **digital**. Each one of these digits, though in binary code, represent the approximate amplitude of the signal sample at that instant.

In Pulse Code Modulation, the message signal is represented by a sequence of coded pulses. This message signal is achieved by representing the signal in discrete form in both time and amplitude.

Basic Elements of PCM

The transmitter section of a Pulse Code Modulator circuit consists of **Sampling, Quantizing** and **Encoding**, which are performed in the analog-to-digital converter section. The low pass filter prior to sampling prevents aliasing of the message signal.

The basic operations in the receiver section are **regeneration of impaired signals, decoding,** and **reconstruction** of the quantized pulse train. Following is the block diagram of PCM which represents the basic elements of both the transmitter and the receiver sections.



Low Pass Filter

This filter eliminates the high frequency components present in the input analog signal which is greater than the highest frequency of the message signal, to avoid aliasing of the message signal.

Sampler

This is the technique which helps to collect the sample data at instantaneous values of message signal, so as to reconstruct the original signal. The sampling rate must be greater than twice the highest frequency component **W** of the message signal, in accordance with the sampling theorem.

Quantizer

Quantizing is a process of reducing the excessive bits and confining the data. The sampled output when given to Quantizer, reduces the redundant bits and compresses the value.

Encoder

The digitization of analog signal is done by the encoder. It designates each quantized level by a binary code. The sampling done here is the sample-and-hold process. These three sections (LPF, Sampler, and Quantizer) will act as an analog to digital converter. Encoding minimizes the bandwidth used.

Regenerative Repeater

This section increases the signal strength. The output of the channel also has one regenerative repeater circuit, to compensate the signal loss and reconstruct the signal, and also to increase its strength.

Decoder

The decoder circuit decodes the pulse coded waveform to reproduce the original signal. This circuit acts as the demodulator.

Reconstruction Filter

After the digital-to-analog conversion is done by the regenerative circuit and the decoder, a low-pass filter is employed, called as the reconstruction filter to get back the original signal.

Hence, the Pulse Code Modulator circuit digitizes the given analog signal, codes it and samples it, and then transmits it in an analog form. This whole process is repeated in a reverse pattern to obtain the original signal.

Experiment 2

Amplitude Shift Keying modulator

Aim: To generate and demodulate an amplitude shift keyed (ASK) signal

Intro to Generation of ASK

Amplitude shift keying - ASK - in the context of digital communications is a modulation process, which imparts to a sinusoid two or more discrete amplitude levels. These are related to the number of levels adopted by the digital message.

For a binary message sequence there are two levels, one of which is typically zero. Thus the

modulated waveform consists of bursts of a sinusoid.

Figure 1 illustrates a binary ASK signal (lower), together with the binary sequence which initiated it (upper). Neither signal has been band limited.

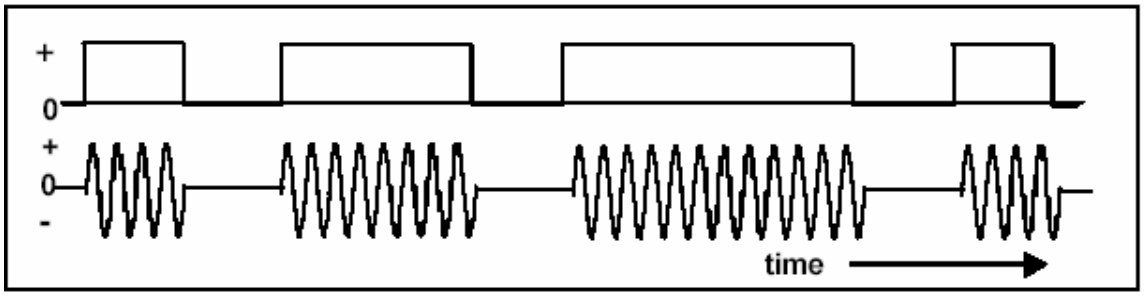


Figure 1: an ASK signal (below) and the message (above)

There are sharp discontinuities shown at the transition points. These result in the signal having an unnecessarily wide bandwidth. Band limiting is generally introduced before transmission, in which case these discontinuities would be 'rounded off'. The band limiting may be applied to the digital message, or the modulated signal itself.

The data rate is often made a sub-multiple of the carrier frequency. This has been done in the waveform of Figure 1.

One of the disadvantages of ASK, compared with FSK and PSK, for example, is that it has not got a constant envelope. This makes its processing (eg, power amplification) more difficult, since linearity becomes an important factor. However, it does make for ease of demodulation with an envelope detector.

Intro to Bandwidth Modification

As already indicated, the sharp discontinuities in the ASK waveform of Figure 1 imply a wide bandwidth. A significant reduction can be accepted before errors at the receiver increase unacceptably. This can be brought about by band limiting (pulse shaping) the message *before* modulation, or band limiting the ASK signal itself *after* generation.

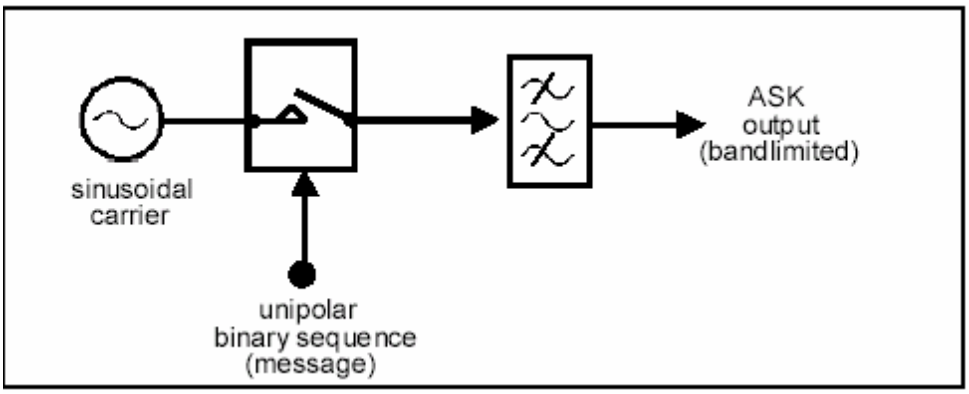


Figure 2: ASK generation method

Figure 3 shows the signals present in a model of Figure 2, where the message has been band limited. The shape, after band limiting, depends naturally enough upon the amplitude and phase characteristics of the band limiting filter.

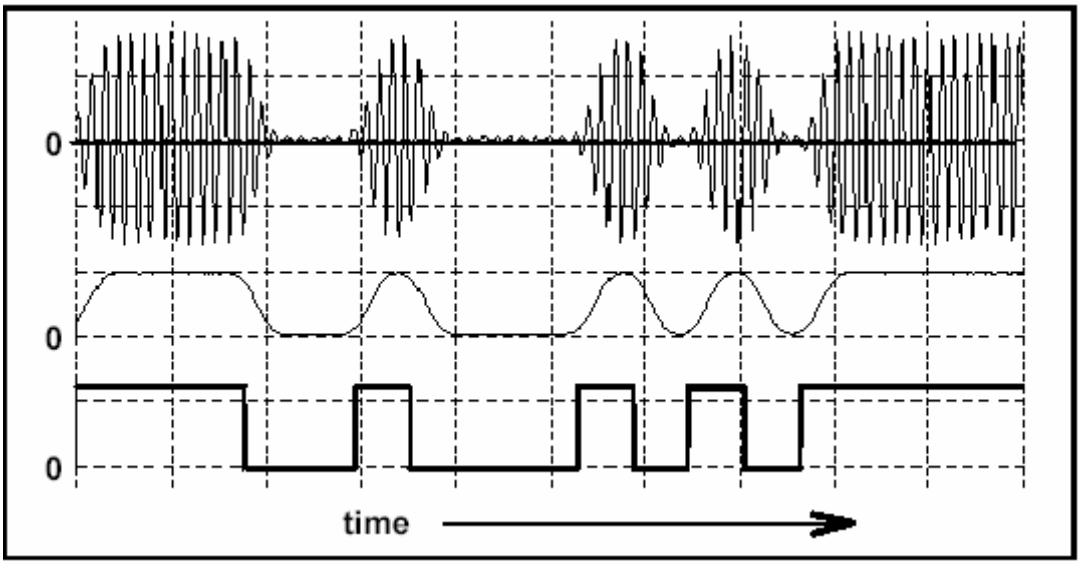


Figure 3: original TTL message (lower), band limited message (center), and ASK (above)

Experiment 3

Amplitude Shift Keying demodulator

Intro to Demodulation

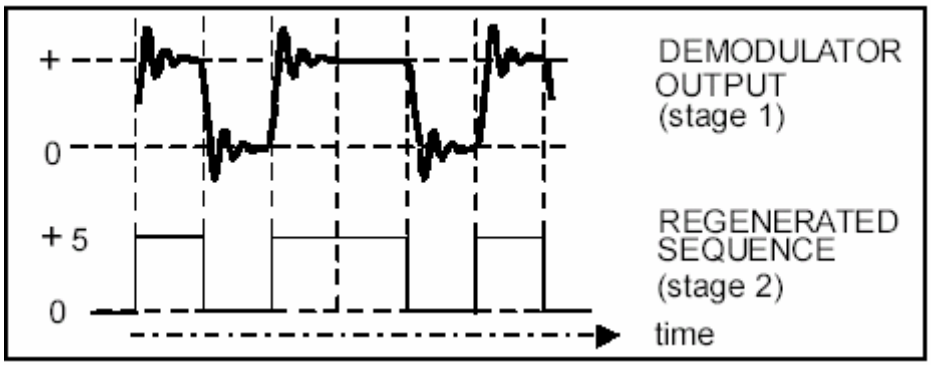
It is apparent from Figures 1 and 4 that the ASK signal has a well-defined envelope. Thus it is amenable to demodulation by an envelope detector.

With band limiting of the transmitted ASK neither of these demodulation methods (envelope detection or synchronous demodulation) would recover the original binary

sequence; instead, their outputs would be a band limited version. Thus further processing by some sort of decision-making circuitry for example - would be necessary. Thus demodulation is a two-stage process:

1. recovery of the band limited bit stream
2. regeneration of the binary bit stream Figure 4 illustrates.

Figure 4: the two stages of the demodulation process



Modeling an ASK Generator

It is possible to model the rather basic generator shown in Figure 2.

The switch can be modeled by one half of a DUAL ANALOG SWITCH module. Being an *analog* switch, the carrier frequency would need to be in the audio range. The TTL output from the SEQUENCE GENERATOR is connected directly to the CONTROL input of the DUAL ANALOG SWITCH. For a synchronous carrier and message use the
8.333 kHz TTL sample clock (filtered by a TUNEABLE LPF) and the 2.083 kHz sinusoidal message from the MASTER SIGNALS module.
If you need the TUNEABLE LPF for band limiting of the ASK, use the sinusoidal output from an AUDIO OSCILLATOR as the carrier. For a synchronized message as above, tune the oscillator close to 8.333 kHz, and lock it there with the sample clock connected to its SYNCH input. This arrangement is shown modeled in Figure 5.

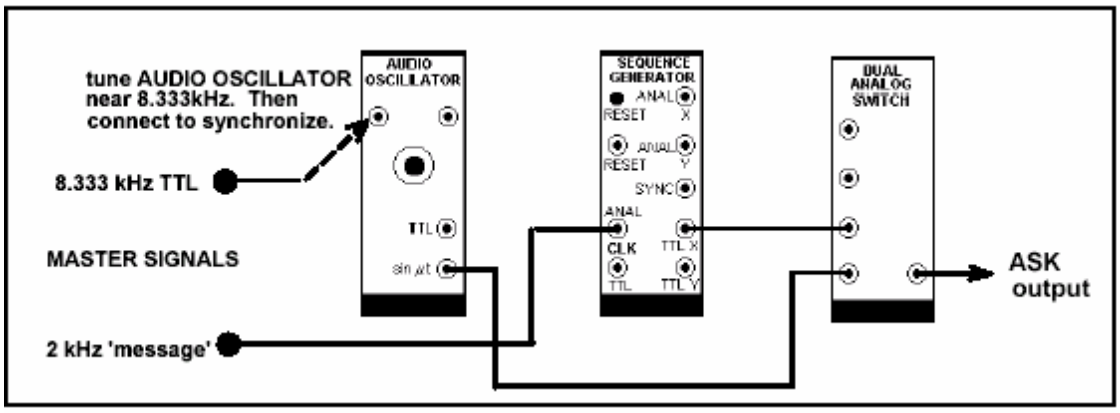


Figure 5: modeling ASK with the arrangement of Figure 2

Demodulation of an ASK signal

Having a very definite envelope, an envelope detector can be used as the first step in recovering the original sequence. Further processing can be employed to regenerate the true binary waveform.

Figure 6 is a model for envelope recovery from a baseband ASK signal.

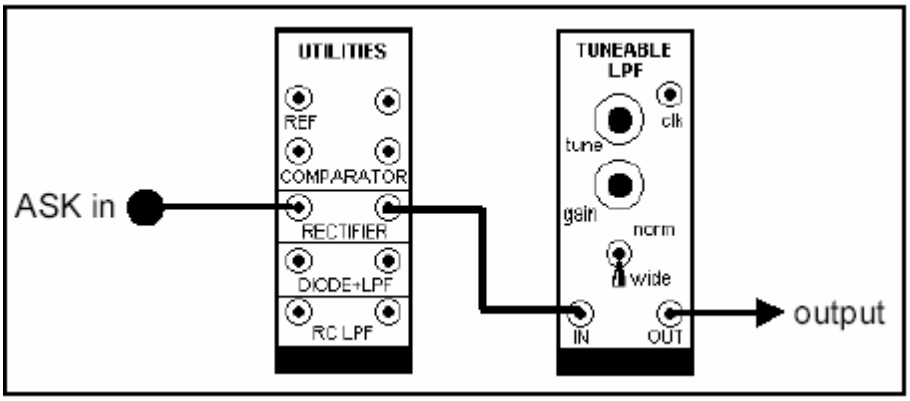


Figure 6: envelope demodulation of baseband ASK

The output from the above demodulators will not be a copy of the binary sequence TTL waveform. Band limiting will have shaped it, as (for example) illustrated in Figure 3.

If the ASK has been band limited before or during transmission (or even by the receiver itself) then the recovered message, in the demodulator, will need restoration (‘cleaning up’) to its original bi-polar format.

Some sort of decision device is then required to regenerate the original binary sequence. This could be done with a COMPARATOR

Experiment 4

Frequency Shift Keying modulator

FSK Generation:

As its name suggests, a frequency shift keyed transmitter has its frequency shifted by the message.

Although there could be more than two frequencies involved in an FSK signal, in this experiment the message will be a binary bit stream, and so only two frequencies will be involved.

The word 'keyed' suggests that the message is of the 'on-off' (mark-space) variety, such as one (historically) generated by a morse key, or more likely in the present context, a binary sequence. The output from such a generator is illustrated in Figure 1 below.

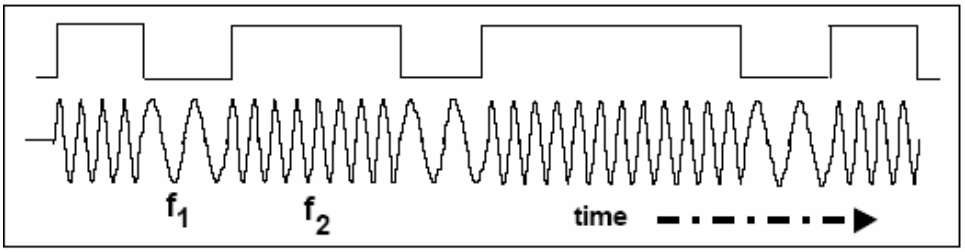


Figure 1: an FSK waveform, derived from a binary message

Conceptually, and in fact, the transmitter could consist of two oscillators (on frequencies f1 and f2), with only one being connected to the output at any one time. This is shown in block diagram form in Figure 2 below.

Unless there are special relationships between the two oscillator frequencies and the bit clock there will

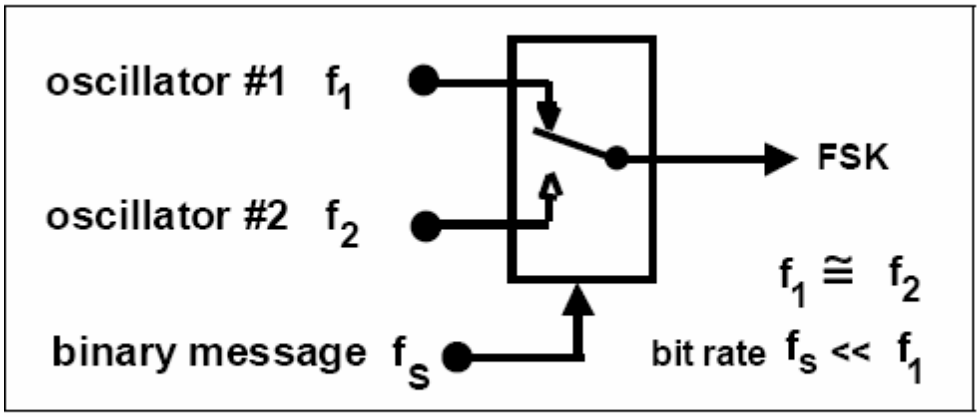


Figure 2: an FSK transmitter

be abrupt phase discontinuities of the output waveform during transitions of the message.

Bandwidth:

Practice is for the tones f1 and f2 to bear special inter-relationships, and to be integer multiples of the bit rate. This leads to the possibility of continuous phase, which offers advantages, especially with respect to bandwidth control.

Alternatively, the frequency of a single oscillator (VCO) can be switched between two values, thus guaranteeing continuous phase - CPFSK.

The continuous phase advantage of the VCO is not accompanied by an ability to ensure that f1 and f2 are integer multiples of the bit rate. This would be difficult (impossible?) to implement with a VCO.

FSK signals can be generated at baseband, and transmitted over telephone lines (for example).
In this case, both f1 and f2 (of Figure 2) would be audio frequencies.
Alternatively, this signal could be translated to a higher frequency. Yet again, it may be generated directly at 'carrier' frequencies.

Experiment 5

Frequency Shift Keying demodulator

Demodulation:

There are different methods of demodulating FSK. A natural classification is into synchronous (coherent) or asynchronous (non-coherent).

Representative demodulators of these two types are the following:

Asynchronous Demodulator:

A close look at the waveform of Figure 1 reveals that it is the sum of two amplitude shift keyed (ASK) signals.
The receiver of Figure 3 takes advantage of this. The FSK signal has been separated into two parts by band pass filters PF) tuned to the MARK and SPACE frequencies.

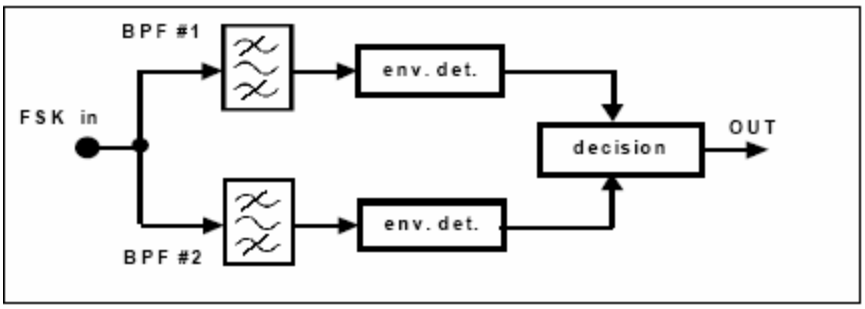


Figure 3: demodulation by conversion-to-ASK

The output from each BPF looks like an amplitude shift keyed (ASK) signal. These can be demodulated asynchronously, using the envelope.

The decision circuit, to which the outputs of the envelope detectors are presented, selects the output which is the most likely one of the two inputs. It also re-shapes the waveform from a band limited to a rectangular form.

This is, in effect, a two channel receiver. The bandwidth of each is dependent on the message bit rate. There will be a minimum frequency separation required of the two tones.

Hint:

You are advised to read ahead, before attempting the experiment, to consider the modeling of this demodulator. Unlike most TIMS models, you are not free to choose parameters - particularly frequencies. If they are to be tuned to different frequencies, then one of these frequencies must be 2.083 kHz (defined as the MARK frequency). This is a restriction imposed by the BIT CLOCK REGEN module, of which the BPF are sub- systems. As a result of this, most other frequencies involved are predetermined. Make sure you appreciate why this is so, then deciding upon:

- bit clock rate
- SPACE frequency
- envelope detector LPF characteristics

Synchronous Demodulator:

In the block diagram of Figure 4 two local carriers, on each of the two frequencies of the binary FSK signal, are used in two synchronous demodulators. A decision circuit examines the two outputs, and decides which is the most likely.

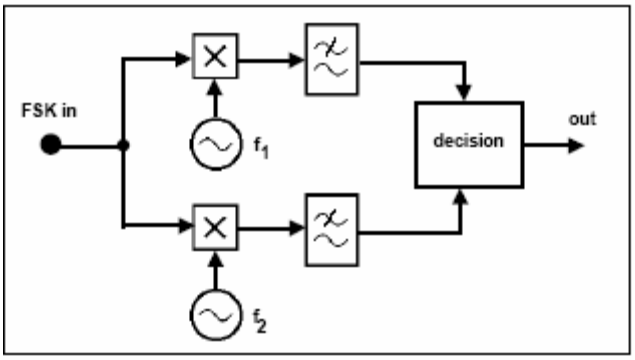


Figure 4: synchronous demodulation

This is, in effect, a two channel receiver. The bandwidth of each is dependent on the message bit rate. There will be a minimum frequency separation required of the two tones. This demodulator is more complex than most asynchronous demodulators.

Phase Locked Loop:

A phase locked loop is a well-known method of demodulating an FM signal. It is thus capable of demodulating an FSK signal. It is shown, in block diagram form, in Figure 5 below.

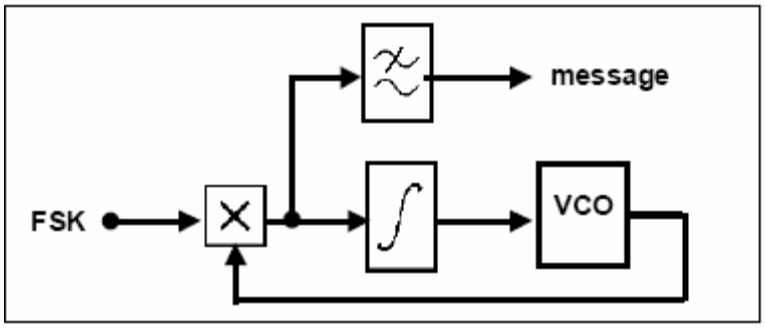


Figure 5: phase locked loop demodulator

The control signal, which forces the lock, is a band limited copy of the message sequence. Depending upon the bandwidth of the loop integrator, a separate LPF will probably be required (as shown) to recover the message.

Experimental Procedure:

Generation:

Scheme #1:

A VCO module is ideally suited for the generation of a continuous phase FSK signal, as shown in Figure 6.

In FSK mode the VCO is keyed by the message TTL sequence. Internal circuitry results in a TTL HI switching the VCO to frequency f1, while a TTL LO switches it to frequency f2. These two frequencies may be in the audio range (front panel toggle switch LO), or in the 100 kHz range (front panel toggle switch HI).

The frequencies f1 and f2 are set by the on-board variable resistors RV8 and RV7 respectively, while a continuous TTL HI or a TTL LO is connected to the DATA input socket.

In FSK mode neither of the front panel rotary controls of the VCO is in operation.

Scheme # 2:

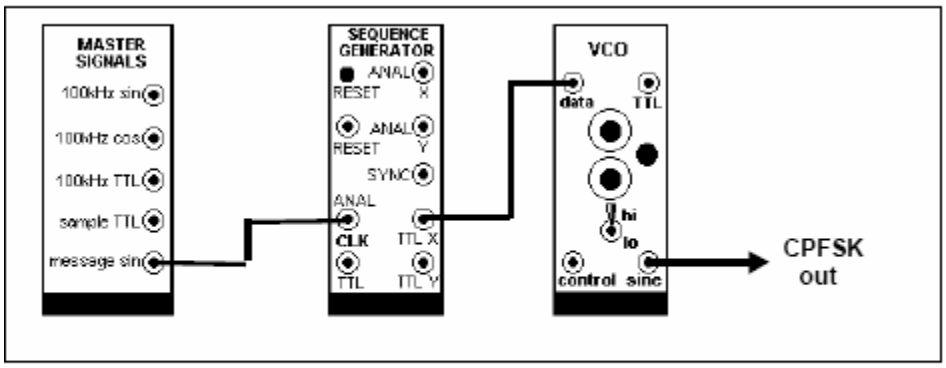


Figure 6: CPFSK

Figure 7 shows a model of the arrangement of Figure 2. It switches either one of two tones to the output, in response to the message sequence.

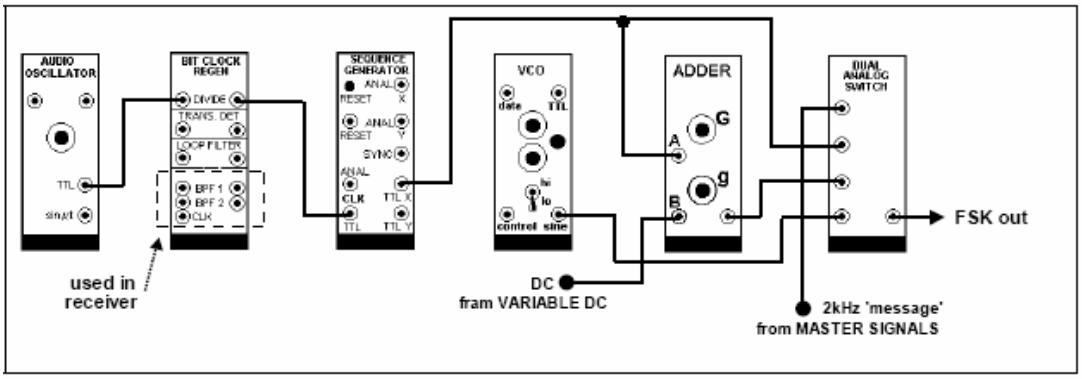


Figure 7: a model of the arrangement of Figure 2

The binary sequence is shown clocked by a divided-by-8 version of the output of an AUDIO OSCILLATOR. This oscillator cannot itself be tuned to this relatively low (for TIMS) frequency. The DIVIDE-BY-8 sub-system is in the BIT CLOCK REGEN module (set the on-board switch SW2 with both toggles DOWN).

The signals at f1 and f2 are provided by the 2.083 kHz MESSAGE from the MASTER SIGNALS module, and a VCO, respectively. The DUAL AUDIO SWITCH module is used to switch between them.

- one of the two ANALOG SWITCHES is driven directly by the TTL binary message sequence.

- the other ANALOG SWITCH is driven by the same TTL sequence, reversed in polarity, and then DC shifted by +5 volts. The reversal and DC shift is performed by the ADDER, with a maximum -ve output from the VARIABLE DC module. Although 5 volt signals exceed the TIMS ANALOG REFERENCE LEVEL the ADDER design is such that it will not be overloaded.

Demodulator:

An example of this is the demodulator of Figure 3, shown modeled in Figure 8.

The demodulator requires two band pass (BPF) filters, tuned to the MARK and SPACE frequencies. Suitable filters exist as sub-systems in the BIT CLOCK REGEN module.

To prepare the filters it is necessary to set the on-board switch SW1. Put the left hand toggle UP, and right hand toggle DOWN. This tunes BPF1 to 2.083 kHz, and BPF2 anywhere in the range 1 <fo< 5 kHz, depending on the VCO (the filter centre frequency will be 1/50 of the VCO frequency).

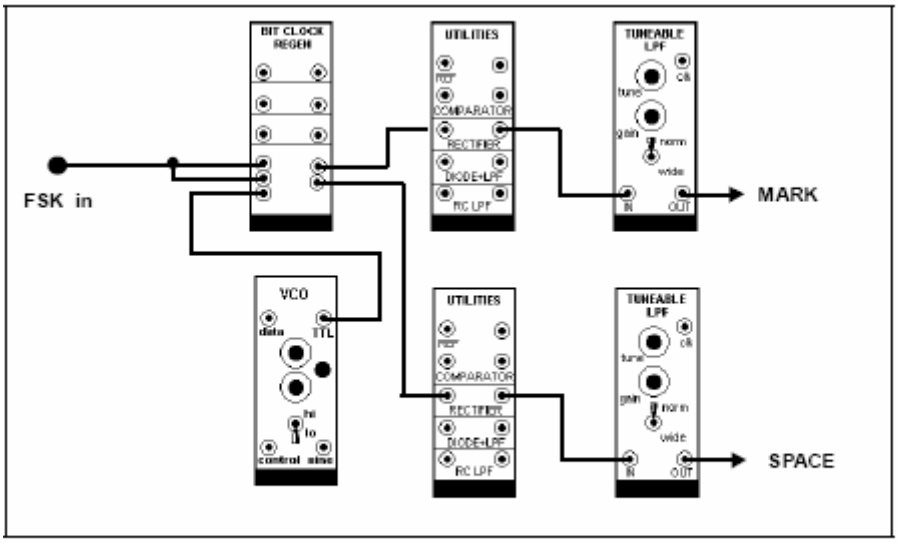


Figure 8: a model of the receiver of Figure 3

If you do not have extra UTILITIES and TUNEABLE LPF modules, then complete just one arm of the demodulator.

Alignment requires the BPFs to be tuned to the MARK and SPACE frequencies. The first is already done (2.083 kHz is already pre-set with SW1); the other is set with the VCO (already pre-set with SW2).

Note that the specified bit rate is, by TIMS standards, rather low. The average oscilloscope display can be a little flicker. Use a short sequence, and the SYNC signal from the SEQUENCE GENERATOR to ext. trig.

Phase Locked Loop:

A phase locked loop is shown in block diagram form in Figure 5, and modeled in Figure 9.

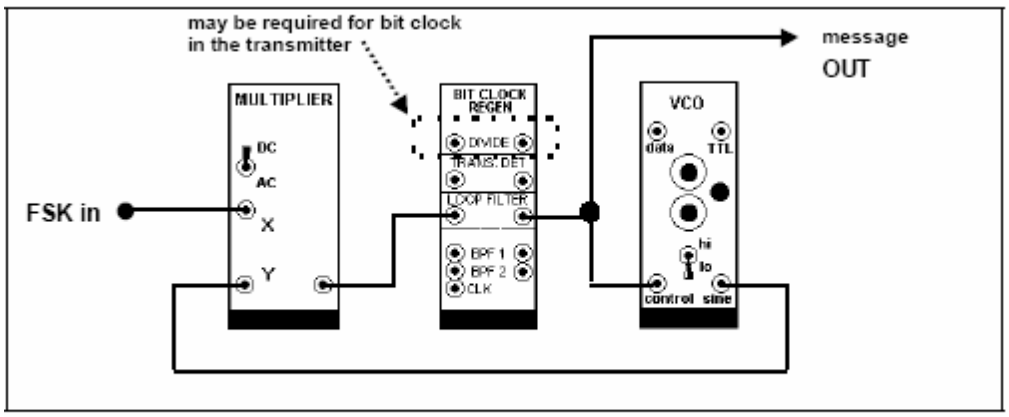


Figure 9: PLL demodulator - the model of Figure 5

For the present experiment the integrator (of Figure 5) is modeled with the LOOP FILTER in the BIT CLOCK REGEN module. This module contains four independent sub-systems. The DIVIDE-BY-8 sub system may already be in use at the transmitter.

EXPERIMENT 6

Phase Shift Keying modulator

Objectives

- To describe the PSK modulation and demodulation
- To carry out a PSK connection, with absolute modulation
- To examine the noise effect on the connection

Material

• Power unit PSU

• Module holder base

• Individual Control UnitSIS1

• Experiment moduleMCM31

• Oscilloscope

THEORETICAL NOTIONS

Phase Shift Keying - PSK

In this kind of modulation, the sine carrier takes 2 or more phase values, directly determined by the binary data signal (2-phase modulation) or by the combination of a certain number of bits of the same data signal (*N*-phase modulation).

In 2-phase PSK modulation, called 2-PSK, or Binary PSK (BPSK), or Phase Reversal Keying (PRK), the sine carrier takes 2 phase values, determined by the binary data signal (fig.1). A modulation technique is the one using a balanced modulator. The output sine-wave of the modulator is the direct or inverted (i.e. shifted of 180°) input carrier, as function of the data signal.

Constellation Diagram

The modulation states of the PSK Modulator are represented with points in a vectorial diagram. Each point is a modulation state, characterized by a phase and an amplitude. This representation is called *constellation diagram*, or more simply *constellation*.

Main aspects

The main aspects characterizing the 2-PSK are:

- use of digital radio transmission
- it requires circuits of average-high complexity
- high possibility of error but lower than the FSK
- if *F*b is the bit transmission speed, the minimum spectrum *Bw* of the modulated signal is higher than *F*b
- the transmission efficiency, defined as the ratio *F*b and *Bw*, is lower than1
- the *Baud* or *Baud rate*, defined as the Modulation speed or symbol speed, is equal to the transmission speed *F*b.

2-PSK Modulator

The block diagram of the 2-PSK modulator is shown in fig.2. The sine carrier (1200 Hz) is applied to an input of the balanced modulator 1; a data signal (indicated with I) is applied to the other input. The circuit operates as balanced modulator, and multiplies the two signals applied to the inputs. Across the output, the sine carrier is direct when the data signal is to low level (bit "0"), inverted (shifted 180°) when the bit is "1". The 2- PSK signal then enters the adder, used for FSK/QPSK/QAM modulations, and exits via a separator stage. The 6dB attenuator makes the signal amplitude half, and is activated only by the QAM. To block the operation of the balanced modulator 2 in 2-PSK mode, the data input of the modulator 2 must be set to J3=b.

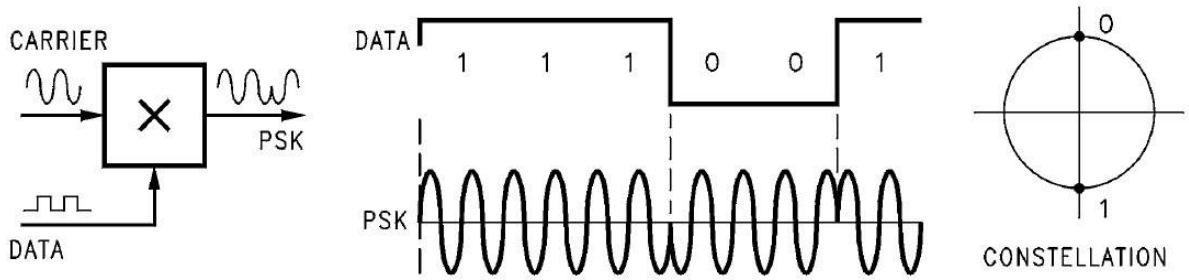


Figure 1: 2-PSK Modulation

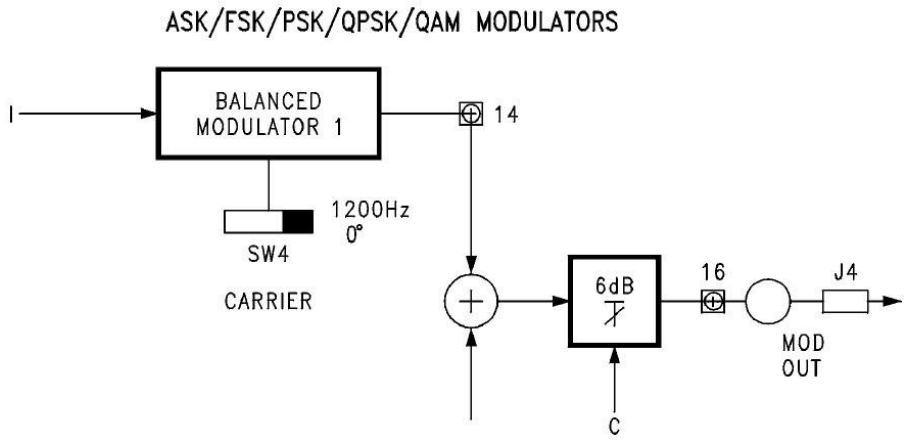


Figure 2: 2-PSK Modulator mounted on the module

EXPERIMENT 7

Phase Shift Keying demodulator

PSK Demodulation with Carrier Regenerator

The demodulation (fig.3) is carried out via a product demodulator, which is reached by the PSK signal and a locally regenerated carrier. This must have the same frequency and phase of the one used in transmission (it must be *coherent* with the received signal), and is taken from the PSK signal as described further on.

Mathematically, the demodulation process is developed as follows. Consider:

- $+\sin(w_C \cdot t)$ = instant PSK signal corresponding to the data bit "1", with $f_C = w_C/2\pi$ carrier frequency
- $-\sin(w_C \cdot t)$ = PSK signal corresponding to the bit"0"
- $\sin(w_C \cdot t)$ = regenerated carrier

When the PSK signal is $+\sin(w_C \cdot t)$ the demodulator supplies:

$[\sin(w_C \cdot t)] \cdot [\sin(w_C \cdot t)] = \sin^2(w_C \cdot t) =$

$= \frac{1}{2} \cdot [1 - \cos(2w_C \cdot t)] = \frac{1}{2} - \frac{1}{2} \cdot \cos(2w_C \cdot t)]$

and contains a d.c. component ($+\frac{1}{2}$) and an a.c. component with double frequency than the carrier $[\cos(2w_C \cdot t)]$. The alternate component can be removed with the low pass filter, and a positive voltage remains which represents the bit "1".

When the PSK signal is $-\sin(w_C \cdot t)$ the demodulator supplies:

$[-\sin(w_C \cdot t)] \cdot [\sin(w_C \cdot t)] = -\sin^2(w_C \cdot t) =$

$= -\frac{1}{2} \cdot [1 - \cos(2w_C \cdot t)] = -\frac{1}{2} + \frac{1}{2} \cdot \cos(2w_C \cdot t)]$

The a.c. component is removed and a negative voltage remains which represents the bit "0".

Carrier regenerator with quadratic law

The carrier regenerator circuit must extract a signal *coherent* (same frequency and phase) with the carrier from the PSK signal. A method used is the one of fig.3:

- a squarer circuit removes the 180° phase shifts in the modulated carrier, to facilitate the same carrier regeneration by the next PLL circuit
- the PLL circuit generates a square-wave signal with double frequency than the PSK carrier
- a phase shifter circuit enables to properly adjust the phase of the regenerated carrier
- a frequency divider divides by 2 the square-wave supplied by the PLL, and provides there generated carrier in this way.

Demodulator circuit

The block diagram of the 2-PSK demodulator with coherent detector is shown in fig.4. It includes the following circuits:

- the carrier regenerator, which supplies a signal coherent (same frequency and phase) with the carrier of the PSK signal. It consists of:
  - a double squarer, which purpose is to remove the 180° phase shifts in the modulated carrier, to facilitate the same carrier regeneration by the next PLL circuit
  - a PLL circuit, which generates a square-wave signal with frequency four times the one of the PSK carrier
  - a frequency divider by 4, to obtain the regenerated carrier. The double squarer and the frequency divider by 4 enables the use of the same circuit for carrier regeneration in the 4-PSK systems too.
- The 2-PSK demodulator (shown in the diagram as DEM I), consists in a double sampler. If the regenerated carrier phase is correct, the sampler output will contain only positive half-waves when the 2- PSK signal has a certain phase, only negative half-waves when the phase is reversed
- a low pass filter
- a squarer circuit (with output in TP29 in case of asynchronous data, which are not re-timed)
- a clock extraction and data re-timing circuit, in case of synchronous data (data output onTP31, clock onTP33).

The filter, the clock extraction and the data re-timing circuit are used to demodulate other kinds of signals, too.

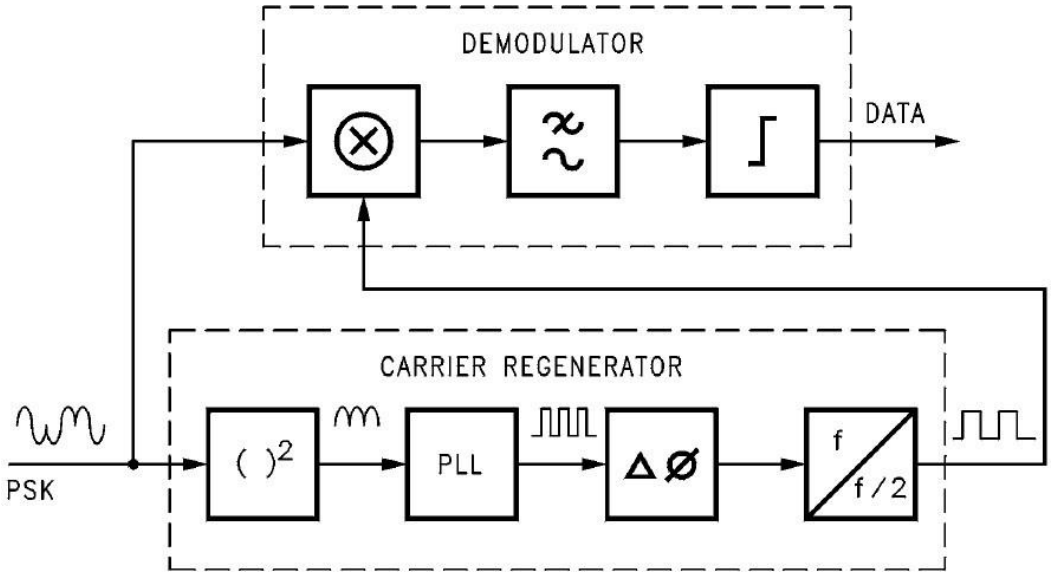


Figure 3: 2-PSK Demodulation with carrier regenerator with quadratic law

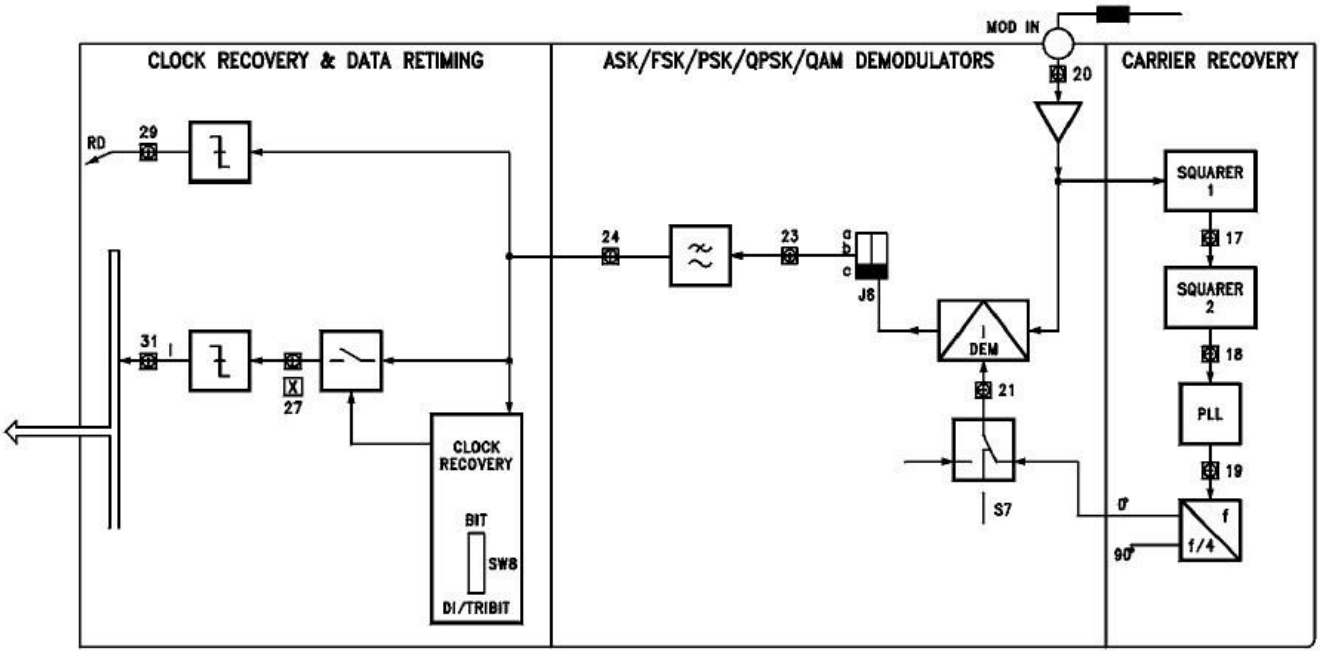


Figure 4: 2-PSK Demodulator mounted on the module

PROCEDURE

Wave-forms of the 2-PSK Modulator

- MCM31 – Disconnect all jumpers
- SIS1 – Turn OFF all switches
- Power the module
- Set the circuit in 2-PSK mode, with 24-bit data source and without data coding (connect J1c-J3b-J4-J5- J6c, set SW2 = Normal, SW3=24 bit, SW4 = 1200, SW=PSK, SW7 = Squaring Loop, SW8 = BIT,ATT
  = min, NOISE = min.
- set an alternated data sequence **00/11** and push **START**
- connect the oscilloscope to **TP6** and **TP16** and examine the data signal and the 2-PSK signal. Adjust the phase (PHASE) to invert the phase of the carrier in correspondence to $\mathbf{0^0}$.

Wave-forms of the 2_PSK demodulator

- Keep the last conditions (connect J1c-J3b-J4-J5-J6c, set SW2 = Normal, SW3=24 bit, SW4 =1200, SW=PSK, SW7 = Squaring Loop, SW8 = BIT, ATT = min, NOISE =min.
- set an alternated data sequence **00/11** and push **START**
- connect the oscilloscope to TP16 and TP20, to examine the PSK signal before and after the communication Channel (Fig.5)
- observe the effect of the communication channel on the PSK signal. As the communication channel is limited band, the phase transitions of the output PSK signal are slightly beveled.
- The PSK demodulator (indicated on the diagram as I_ DEM), consists in a double sampler, which samples the negative and positive half-wave of the incoming PSK signal. The sampling clock consists in the carrier regenerated by the *Carrier Recovery Section*
- Across TP21 you can note a rectangular signal which samples the negative half-wave of the PSK signal. The frequency of the sampling signal is equal to the frequency of the PSK carrier (1200 Hz), the sampling duration is equal to ¼ the period.

Q2 What kind of signal can you observe on the demodulator output (TP23)?

- The signal supplied by the PSK demodulator passes a low filter, which eliminates the residuals of the 1200 Hz carrier. Across the filter's output (TP24, Fig. 5) you get the wave-form of the detected data signal.
- It can happen that the received signals are inverted in respect to the transmitted one. This can be understood as the demodulator does not know which of the coming phases is 0^0 or 180^0, and this ambiguity can take to the inversion of the demodulated data. The ambiguity is overcome by carrying out a data differential coding before the modulation. In case push ***Phase Sync*** to obtain data with proper sign.
- The squared data signal can be detected across TP31. See on the oscilloscope the correspondence between the transmitted data (TP6) and the received ones(TP31)
- Across TP32 see the reception clock (rectangular wave at 600 Hz), reconstructed starting from the data signal and used to re-time the same data.

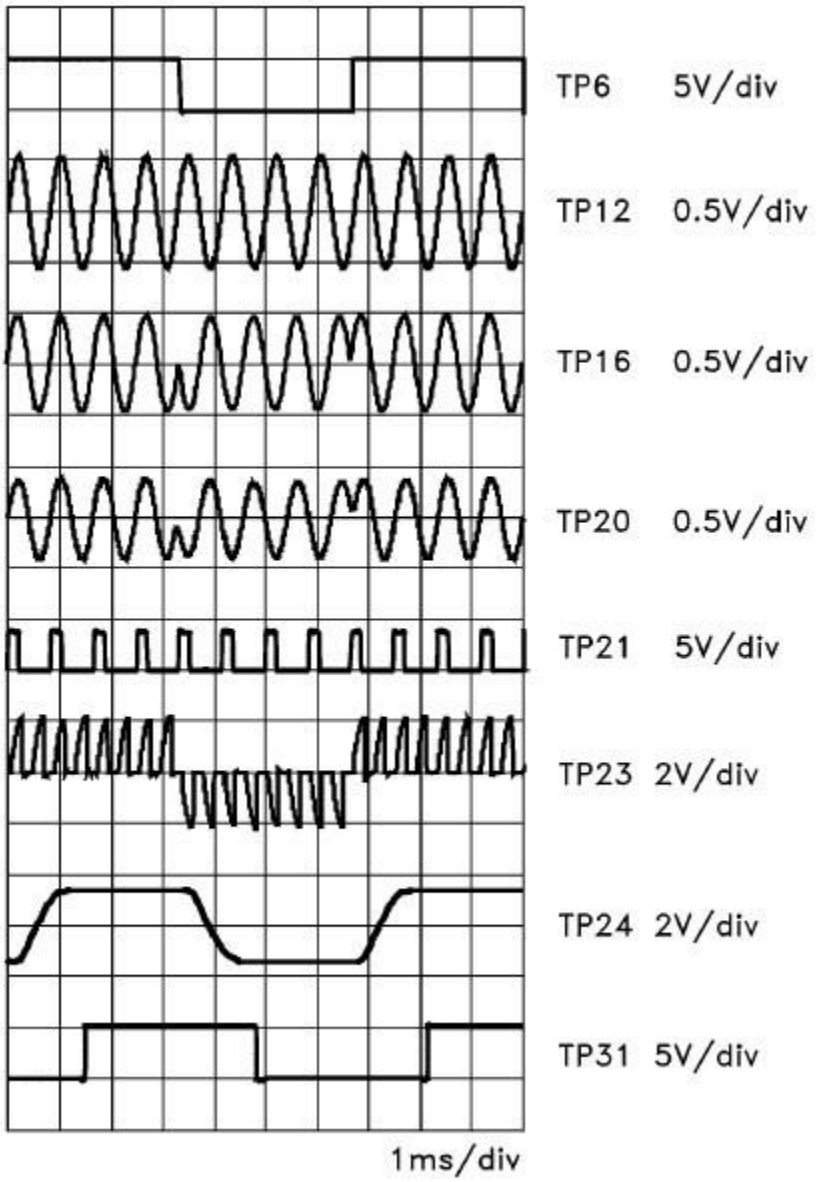


Figure 5: 2-PSK Waveforms

- SIS1 - Turn ON switchS24

- SIS1 - Turn OFF switchS24
- Set now a data sequence with few alternation, e.g. all “1” and a single “0”, and push **START**
- Examine the signal across TP4 (transmitted data), TP31 (received data), TP32 (reception clock). Eventually push *Phase Sync* to obtain the data with proper sign acrossTP31.
- It can happen that the reception clock (TP32) is not stable, and that the received data (TP31) has some time different from the transmitted (TP4). This is due to a bad operation of the PLL which regenerates the reception clock.
- The Manchester coding of the data to be transmitted ensures there are always alternates in the transmitted signal, facilitating in this way the clock extraction by the PLL.
- Supply the 2-PSK modulator with the Manchester coded data (disconnect J1c and connectJ1-d)
- The Received Data and the Reception Clock are now available after the Manchester coder (TP9and TP10)
- Keep the same data sequence of the last case and see that:
  - The clock is now regenerated properly
  - The received data is equal to the transmitted ones

Experiment 8

Line coding encoder-decoder

Curriculum Objectives

1.To understand the theory and applications of line code encoder.
2.To understand the encode theory and circuit structure of NRZ.
3.To understand the encode theory and circuit structure of RZ.
4.To understand the encode theory and circuit structure of AMI.
5.To understand the encode theory and circuit structure of Manchester.

1-1 : Curriculum Theory

Line coding is a part of source coding. Before PCM signal send to modulator, we use certain s signal mode in certain application. The considerations of selecting the digital signal modes to carry the binary data are: 1. types of modulation, 2. types of demodulation, 3. the limitation of bandwidth, and 4 types of receiver.

Line coding can be divided into two types, which are return-to-zero (RZ) and no return-to-zero (NRZ). RZ line coding denotes for a single bit time (normally is half of a single bit time), the waveform will return to 0 V between data pulses.

The data stream is shown in figure 1-1(c). NRZ line coding denotes for a singlebit time, the waveform will not return to 0 V. The data stream is shown in figure1-1(a). As a result of the characteristics of signal, line coding also can be divided into two types, which are unipolar signal and bipolar signal. Uni-polar signal denotes that the signal amplitude varies between a positive voltage level which are +V and 0 V. The only different between bipolar signal and unipolar signal is the signal amplitude varies between a positive and a negative voltage level which are +V and -V. Figure 1-1 shows different types of line code signals and we will discuss the encoding signals in next section.

1. . Uni-polar No return- to- zero Signal Encode

The data stream of unipolar nonreturn-to-zero (UNI-NRZ) is shown in figure 1-1(a). From figure 1-1(a), when the data bit is "1", the width and the gap between bits of UNI-NRZ are equal to each other's; when the data bit is "0", then the pulse is represented as 0V. The circuit diagram of UNI-NRZ encoder is shown in figure 1-2. As a result of the data signal and the NRZ encoder signal are similar, therefore, we only need to add a buffer in front of the circuit.

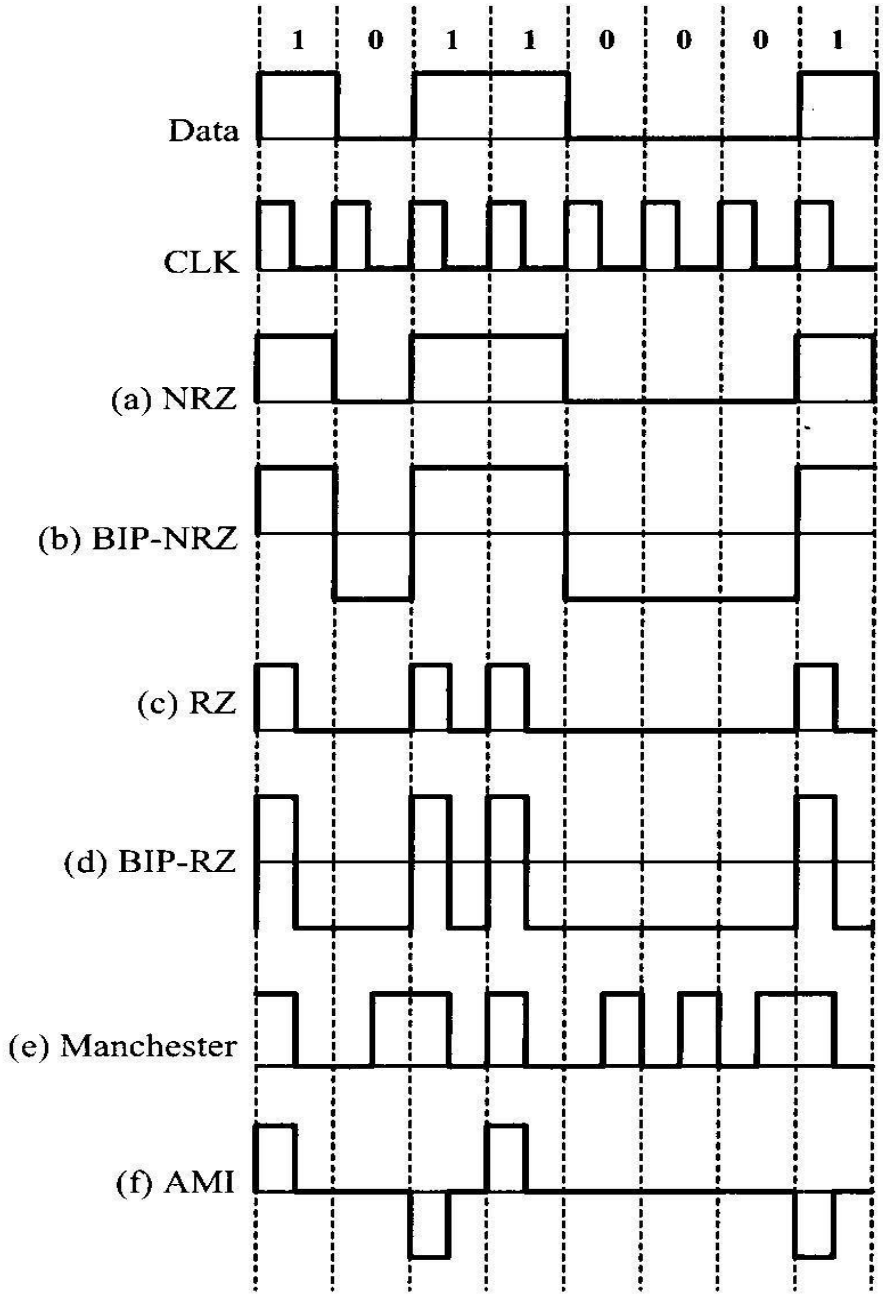


Figure 1-1 Different types of line code signal waveforms.

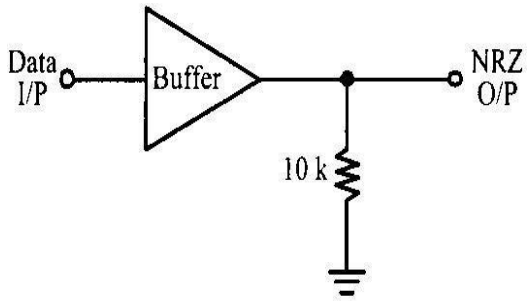


Figure 1-2 Circuit diagram of unipolar nonreturn-to-zero encoder.

2 Bipolar Non return-to-zero Signal Encode

The data stream of bipolar nonreturn-to-zero (BIP-NRZ) is shown in figure 1-1(b). When the data bit of BIP-NRZ is "1" or "0", the signal amplitude will be a positive or a negative voltage level. As for bit time, no matter the data bit is "1" or "0", the voltage level remains same. Figure 1-3 is the circuit diagram of BIP-NRZ encoder. By comparing the data streams of UNI-NRZ a BIP-NRZ, the only difference is the signal amplitude is a negative voltage level when the data bit is"0", therefore, we may utilize a comparator to encode the data bit in the circuit.

3 Unipolar Return-to-zero Signal Encode

The data stream of unipolar return-to-zero (UNI-RZ) is shown in figure 1-1(c). When the data bit is "1", the signal amplitude at 1/2-bittime is positive voltage level and the rest of the bit time is represented as 0 V. When the data bit is "0", there is no pulse wave that means the signal amplitude is 0 V. The bit time of RZ is half of the bit time of NRZ, therefore, the required bandwidth of RZ is one time more than NRZ. However, RZ has two phase

variations in a bit time, which is easy for receiver synchronization. From figure 1-1, compare the data signal, clock signal and data after encoding, we know that in order to obtain the encoding data of RZ, we need to "AND" the data signal and clock signal. The circuit diagram of unipolar return-to-zero encoder is shown in figure 1-4.

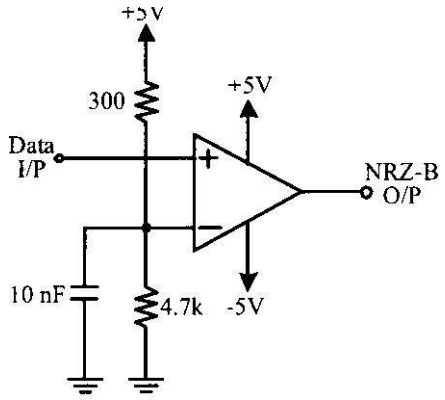


Figure 1-3 Circuit diagram of bipolar nonreturn-to-zero encoder.

Figure 1-4 Circuit diagram of unipolar return-to-zero encoder.

4. Bipolar Return-to-zero Signal Encode

The data stream of bipolar return-to-zero (B1P-RZ) is shown in figure 1-1(d). When the data bit is "1", the signal amplitude at 1/2-bit time is positive voltage level and the other 1/2-bittime is negative voltage level. When the data bit is "0", the signal amplitude of the bit time is represented as negative voltage level. Figure 1-5 is the circuit diagram of BIP-RZ. By comparing the data streams of RZ and BIP-RZ in figure 1-1, we only need a converter to convert the encoding signal from unipolar to bipolar, therefore, we utilize a comparator to design the converter, which can convert the RZ signal to BIP-RZ signal.

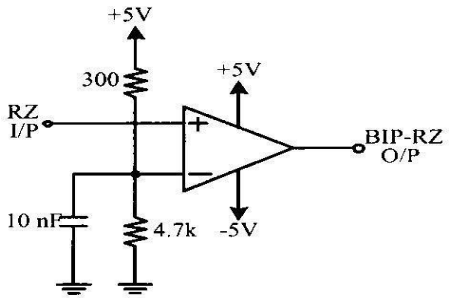


Figure 1-5 Circuit diagram of bipolar return-to-zero encoder.

5. Alternate Mark Inversion Signal Encode

Alternate mark inversion (AMI) signal is similar to RZ signal except the alternate "1" inverted. The data stream of AMI signal is shown in figure 1-1(f). When the data bit is "1", the first signal amplitude at 1/2-bittime is positive voltage level and the other 1/2-bittime is 0 V; then the second signal amplitude at 1/2-bit time is negative voltage level and the other 1/2-bittime 0 V, therefore, the only different between AMI and RZ is the alternate "1 " are inverted. When the data bit is "0", the signal amplitude is 0V. This type of encode is common used by telephone industry which is pulse coding modulation (PCM).

Figure 1-6 is the circuit diagram of AMI signal encode. In order to obtain the AMI, encode signal, the data and clock signals need to pass through the buffer stage,
which is comprised by a pair of transistors and NOT gates. After that we need to "AND" the output of data signal and clock signal, then pass through a divider circuit by
utilizing clock as switch exchange. The final signal is the AMI signal. The minimum bandwidth of AMI is less than UNI-RZ and BIP-RZ. An additional advantage of AMI is the transmission errors can be detected by detecting the violations of the alternate-one rule.

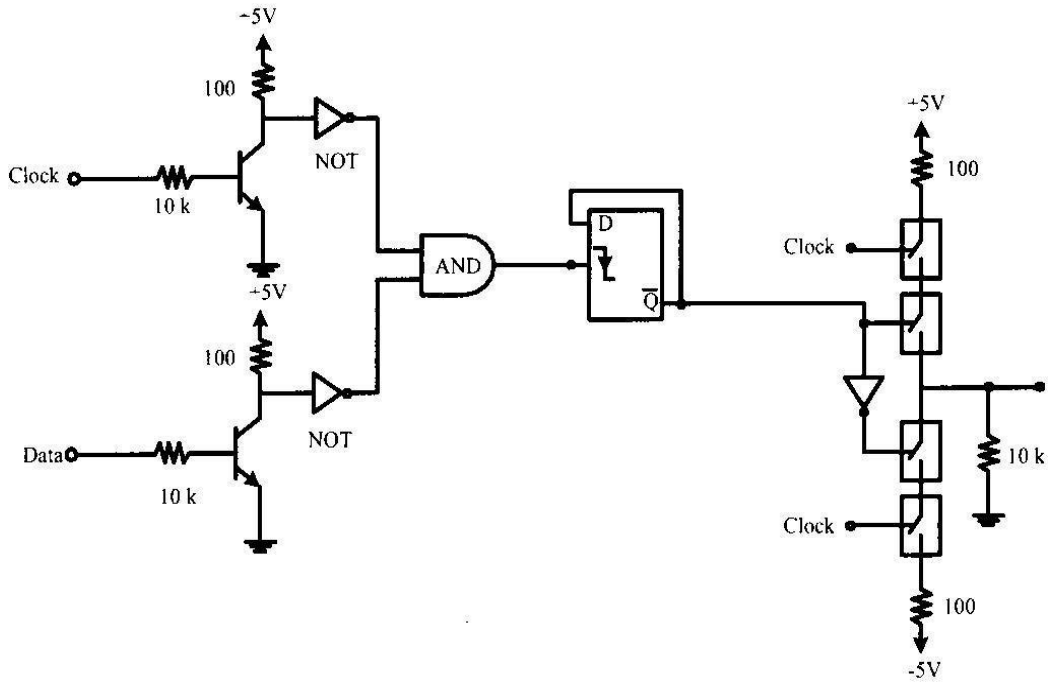


Figure 1-6 Circuit diagram of AMI signal encoder.

6. Manchester Signal Encode

Manchester signal is also known as split-phase signal. The data stream of Manchester signal is shown in figure 1-1(e). When the data bit is "1", the signal amplitude at first 1/2-bittime is positive voltage level and the other 1/2-bittime is negative voltage level. When the data bit is "0", the signal amplitude at first 1/2 -bit time is negative voltage level and the other 1/2-bit time is positive voltage level. This type of encode signal has the advantage of memory, therefore, the required bandwidth is larger than the other encode signals. So, it is suitable applied to network such as Ethernet. From figure 1-1, compare the data signal, clock signal and data after encoding, we know that in order to obtain the encoding data of Manchester, we need to "XNOR" the data signal and clock signal. Figure 1-7 is the circuit diagram of Manchester signal encoder.

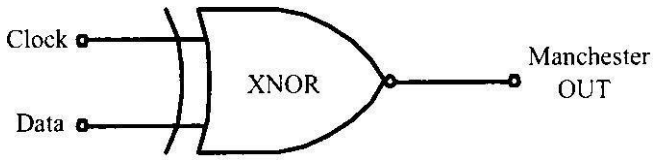


Figure 1-7 Circuit diagram of Manchester signal encoder.

1-2 : Experiment Items

Experiment 1: Unipolar and bipolar NRZ signal encode

Experiment a: Unipolar NRZ signal encode

1. To implement a unipolar NRZ encode circuit as shown in figure 1-2 or refer to figure DCT1-1 on GOTT DCT-6000-01module.

2. Setting the frequency of function generator to 1 kHz TTL signal and connect this signal to the Data I/P. Then observe on the output waveform by using oscilloscope and record the measured results in table1-1.

3. According to the input signals in table 1-1, repeat step 2 and record the measured results in table1-1.

Experiment b: Bipolar NRZ signal encode

1. To implement a bipolar NRZ signal encode circuit as shown in figure 1-3 or refer to figure DCT1-1 on GOTT DCT-6000-01module.

2. Setting the frequency of function generator to 1 kHz TTL signal and connect this signal to the Data I/P. Then observe on the waveforms of TP1 and BIP-NRZ O/P by using oscilloscope and record the measured results in table1-2.

3. According to the input signals in table 1-2, repeat step 2 and record the measured results in table1-2.

Experiment 2: Unipolar and Bipolar RZ signal encode

Experiment a: Unipolar RZ signal encode

1. To implement a unipolar RZ signal encode circuit as shown in figure 1-4 or refer to figure DCT 1-2 on GOTT DCT-6000-01 module.

2. Setting the frequency of function generator to 2 kHz TTL signal and connect this signal to the CLK I/P of figure DCT 1-2 and CLK at the left bottom. After that connect the Data O/P at the left bottom to the Data I/P in figure DCT 1-2. Then observe on the waveforms of CLK I/P, Data I/P and UNI-RZ O/P by using oscilloscope, and record the measured results in table1-3.

3. According to the input signals in table 1-3, repeat step 2 and record the measured results in table1-3.

4. Setting the frequency of function generator to 2 kHz TTL signal and connect this signal to the CLK I/P in figure DCT 1 - 2. Then setting another frequency of function generator to 1 kHz TTL signal and connect this signal to the Data I/P in figure DCT1-2. Then observe on the waveform of CLK I/ P, Data I/P and UNI- RZ O/ P by using oscilloscope, Hid record the measured results in table 1-4.

5. According to the input signals in table 1-4, repeat step 4 and record the measured results in table1-4.

Experiment b: Bipolar RZ signal encode

1. To implement a bipolar RZ signal encode circuit as shown in figure 5 or refer to figure DCT1-2 on GOTT DCT-6000-01module.

2. Setting the frequency of function generator to 2kHz TTL signal and connect this signalto the CLK I/P in figure DCT1-2 and CLK at the left bottom. After that connect the Data O/P at the left bottom to the Data I/P in figure DCT1-2. Then observe on the waveforms of CLK I/P, Data I/P, TP1 and BIP-RZ O/P by using oscilloscope, and record the measured results in table1-5.

3. According to the input signals in table 1-5, repeat step 2 and record the measured results in table1-5.

4. Setting frequency of function generator to 2kHz TTL signal and connect this signal to the CLK I/P in figure DCT1-2. Then setting another frequency of function generator to 1 kHz TTL signal and connect this signal to the Data I/P in figure DCT1-2. Then observe on waveforms of CLK I/P, Data I/P, TP1 and BIP-RZ O/P by using oscilloscope, and record the measured results in table1-6.

5. According to the input signals in table 1-6, repeat step 4 and record the measured results in table1-6.

Experiment c: AMI signal encode

1. To implement an AMI signal, encode circuit as shown in figure 1-6 or refer to figure DCT 1-3 on GOTT DCT-6000-01module.

2. Setting the frequency of function generator to 2 kHz TTL signal and connect this signal to the CLK I/P in figure DCT 1-3 and CLK at the left bottom. After that connect the Data O/P at the left bottom to the Data I/P in figure DCT1-3. Then observe on the waveforms of CLK I/P, Data I/P, TP1, TP2, TP3, TP4, TP5 and AMI O/P by using oscilloscope, and record the measured results in table1-7.

3. According to the input signals in table 1-7, repeat step 2 and record the measured results in table 1-7.

4. Setting the frequency of function generator to 2 kHz TTL signal and connect this signal to the CLK I/P in figure DCT 1-3. Then setting another frequency of function generator to 1 kHz TTL signal and connect this signal to the Data I/Pin figure DCT1-3. Then observe on the waveforms of CLK I/P, Data I/P, TP1, TP2, TP3, TP4, TP5 and AMI O/P by using oscilloscope, and record the measured results in table1-8.

5. According to the input signals in table 1-8, repeat step 4 and record the measured results in table 1-8.

Experiment d: Manchester signal encode

1. To implement a Manchester signal, encode circuit as shown in figure 1-7 or refer to figure DCT1-4 on GOTT DCT-6000-01module.

2. Setting the frequency of function generator to 2 kHz TTL signal and connect this signal to the CLK I/P in figure DCT 1-4 and CLK at the left bottom. After that connect the Data O/P at the left bottom to the Data I/P in figure DCT1-4. Then observe on the waveforms of CLK I/P, Data I/P and Manchester O/P by using oscilloscope, and record the measured results in table 1-9.

3. According to the input signals in table 1-9, repeat step 2 and record the measured results in table1-9.

4. Setting the frequency of function generator to 2 kHz TTL signal and connect this signal to the CLK I/P in figure DCT 1-4. Then setting, another frequency of function generator to 1 kHz TTL signal and connect this signal to the Data I/P in figure DCT 1-4. Then observe on the waveforms of CLK I/P, Data I/P and
Manchester O/P by using oscilloscope, and record the measured results in table 1-10.

5. According to the input signals in table 1-10, repeat step 4 and record the measured results in table1-10