Lab

C1114

كلية الهندسة – جامعة المنصورة

C1114 معمل الدوائر المنطقية

Computer Engineering and Control Systems

قسم هندسة الحاسبات ونظم التحكم

Laboratory Book

COMPUTER ENGINEERING AND CONTROL SYSTEMS DEPARTMENT

2019

C1114 معمل الدوائر المنطقية

Laboratory Book

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Part

1

1: Laboratory Basic Information

أولا : البيانات الأساسية للمعمل

إسم المعمل:	**الحاسبات المصغرة**
القسم العلمي:	**هندسه الحاسبات والنظم**
المشرف:	**ا.م.د./ أحمد صالح.** **د.نهي صقر**
مهندس المعمل:	**م. ماري مينا فؤاد.**
أمين المعمل:	**السيدة/ سلسبيل هلال إبراهيم.**
التليفون:	**داخلي 1492.**
الموقع بالنسبة للكلية:	**الناحية البحرية.**
مساحة المعمل:	**120 متر^2.**

Part 2

2: Laboratory Instruments

ثانياً: قائمة بالأجهزة والمعدات الموجودة بالمعمل

م	إسم الجهاز	العدد	Serial Number
1	**CPU Intel Core 2 Due 2.9/2M**	**23**	**MB ECS-G41 T.M**
2	**CPU Intel P.IV 3 GHz**	**1**	**MB Intel P.IV GB 945 chipset**
3	Digital Kit	**6**	Basic and sequential
4	Digital Kit	**4**	Basic logic
5			
6			

Part

3

3: Laboratory Experimental List

ثالثاً: قائمة بالتجارب التي تؤدي داخل المعمل

م	التجربة	الغرض منها
1	Investigate the operation of R-S flip flop	التعرف على مكونات ووظيفة و كيفية عمل الـ RS .
2	Investigate the operation of T flip flop	التعرف على مكونات ووظيفة و كيفية عمل الـ T Flip flop .
3	Investigate the operation of D flip flop	التعرف على وظيفة و كيفية عمل الـD flip flop .
4	Investigate the operation of J-K flip flop	التعرف على مكونات ووظيفة و كيفية عمل الـ J-K flip flop .
5	Design Sequential Circuits and counters	تصميم الدوائر التتابعية
6	Linux Commands	تنفيذ اوامر اللينكس كنظام تشغيل

Part

4

4: Laboratory Beneficiaries

رابعاً: الخدمات المجتمعية التي يؤديها المعمل:

Part

5

5: Laboratory Student Beneficiaries

خامساً: الخدمات الطلابية التي يؤديها المعمل:

عدد الطلاب المستفيدين من المعمل	في خلال مده اسبوع 200 طالب
الأقسام العلمية المستفيدة من المعمل	قسم هندسة الحاسبات والنظم
الفرق الدراسية المستفيدة من المعمل	الفرقة الاولى – الفرقة الثانية – الفرقة الثالثة من قسم هندسة الحاسبات ونظم التحكم.
المقررات الدراسية التي تستفيد من المعمل	تصميم رقمى و منطقى 1 – تصميم رقمى و منطقى 2 – نظم تشغيل 1.
الأنشطة الطلابية داخل المعمل	ندوات طلابية– عقد جلسات مناقشة حلقات البحث لطلاب تمهيدى الماجيستير و دبلومة الحاسبات – مناقشة مشاريع التخرج لطلاب قسم هندسة الحاسبات و نظم التحكم - عقد جلسات الامتحانات الشفوية لمادة نظم التشغيل – عقد الامتحانات العملية لمادة تصميم رقمى 1 و تصميم رقمى 2 – التدريب الصيفى لطلاب الصف الاول بقسم هندسة الحاسبات و نظم التحكم.
عدد طلاب الدراسات العليا المستفيدين من المعمل	40 طالب ضمن و دبلومة الحاسبات.
عدد الرسائل العلمية التي تمت في المعمل	تطبيق الجزء العملى لبعض رسائل علمية خاصة بالنظم الموزعة و انظمة المتشابكات الحسابية و نظم حماية الشبكات و ذلك خلال (2011 الى 2013).
عدد الدورات التدريبية التي تمت في المعمل	
المسابقات العملية التي شارك فيها طلاب من المستفيدين من المعمل	مسابقات خاصة بمشاريع التخرج الخاصة بطلاب القسم ضمن يوم المهندس المصرى – مؤسسة مصر المحروسة – ايتيدا

Part

6

6: Laboratory Experimental

سادساً: التجارب المعملية

Experiment 1 NOR Gate Circuit

OBJECTIVE

Understanding how to construct other combinational logic gates using NOR gates.

DISCUSSION

The symbol of a NOR gate is shown in Fig. 2-1. The Boolean expression for the N gate is F= A + B; in de Morgan's theorem, F= A + B = A x B.

When A=B, F= A + B = A +A= A. When B=O, F= A + B = A + 0 = A. Therefore, the NOR gate can be used to construct NOT, OR; AND; NAND; and XOR gates. We will not attempt to construct various logic gates in this experiment by connecting NOR gates in different ways.

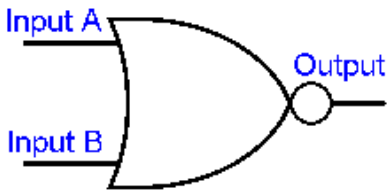


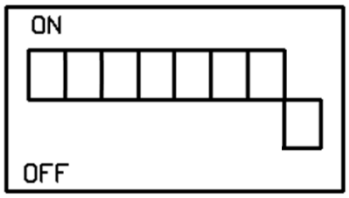
Fig. 2-1 Symbol of NOR gate

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM02

EXERCISE

1. Make sure the Fault Simulator DIP Switch follows the below setting :
2.



3. U1a of Fig. 2-2 (a) will be used to construct a NOT gate.

4. Connect inputs A, B to Data Switches SWO, SW1 and output F1 to Logic Indicator L1. Set SWO to "0", observe states of F1 at SW1="0" and SW1="1 ".

   Does the circuit act as a NOT gate? (As in Fig. 2-2 (b))

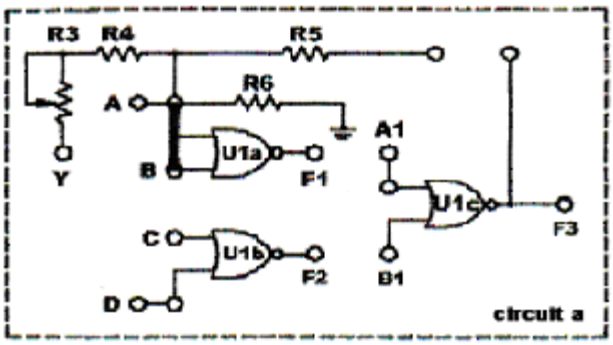


Fig. 2-2 (a) DLLT-EM02: Assembly Logic Circuits (1)

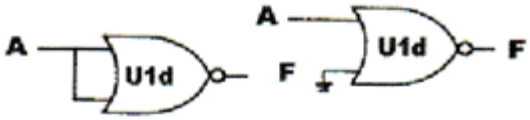


Fig. 2-2 (b) NOR gate used as NOT gate

5. Insert a connection clip between A and B. Connect A to SWO and F1 to L1. What is the state of F1 when SW0=0 and SW0=1?

   Does the circuit act as a NOT gate?

6. Use U 1a and U 1c to construct a buffer shown on the left side of Fig. 2-2 (c). Insert connection clips between A~ B; F1~A1; A1~ B1. Connect input A to SWO and output F3 to L1. What is the state of F3 when SW0=0 and SW0=1?

   Does the circuit act as a buffer?

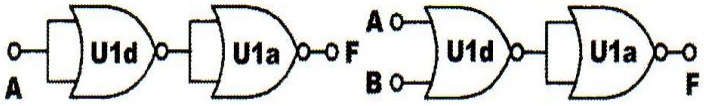


Fig. 2-2 (c) NOR gate use as Buffer and OR gate

7. Use U1a and U1c to construct an OR gate shown on the right side of Fig. 2-2 (c). Insert connection clips between F1 ~A1 and A1~B1. Connect inputs A to SW0, B to SW1; and output F3 to L1. Follow the input sequences shown below and record the output states in Table 2-1.

Table 2-1

8. Insert connection clips according to the figure below. The circuit will act as an AND gate.

(1) Connect A to SW0; D to SW1; F1 to Al; F2 to 131 - F3 to 1-1.
(2) Follow the input sequences given below. Record the output states in Table 2-2.

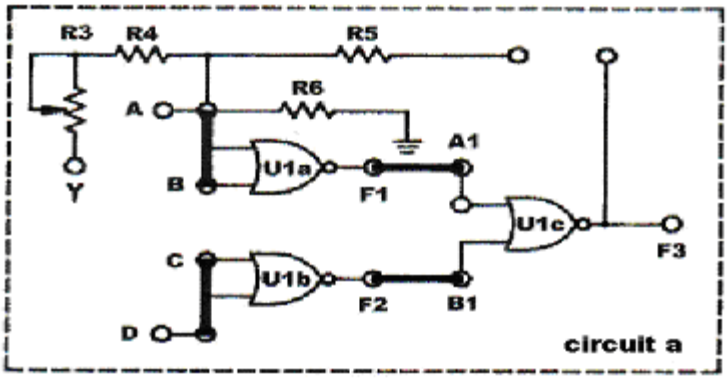


Table 2-2

RESULTS

1. NOR gate can be used to construct just about any basic logic gate.
2. There are two ways to use NOR gate as an inverter. Since TTL gates have higher current when the input is grounded, if TTL NOR gate is to be used as an inverter, its two inputs should be connected together.

FAULT SIMULATION

1. U1a and U1c are used as a buffer and the outputs stay in high state. Try to locate all possible faults.
2. The outputs stay at low state when U1a and U1c are used as a buffer. Try to locate all possible faults.
3. When U1a. U1b. U1c are used as an AND gate, the output F is only affected by the input A What could be the faults?

Experiment 3 NAND Gate Circuit

OBJECTIVE

To understanding how the construct various combinational logic gates with NAND gates.

DISCUSSION

The symbol of a NAND gate is shown in Fig. 2-4. The Boolean expression for a NAND gate is F= $\overline{A \times B}$; in de Morgan's theorem, $\overline{A \times B}$ = A + $\bar{B}$.

When A=B, F= $\overline{A \times B}$ = A. When B=1, F= $\overline{A \times B}$ = $\overline{A \times 1}$ = $\bar{A}$. Like the NOR gates, NAND gates can be used to construct just about any basic logic gates. We will attempt to construct various basic gates in this experiment by connecting NAND gates in different ways.

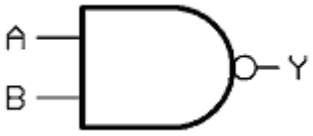


Fig. 2-4 Symbol of NAND gate

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM02: Assembled Logic Circuits (1) Experiment Module

EXERCISE

1. Insert connection clips according to Fig. 2-5(a), using U2c and U2d to construct the NOT gate shown on left side of Fig. 2-5(b).

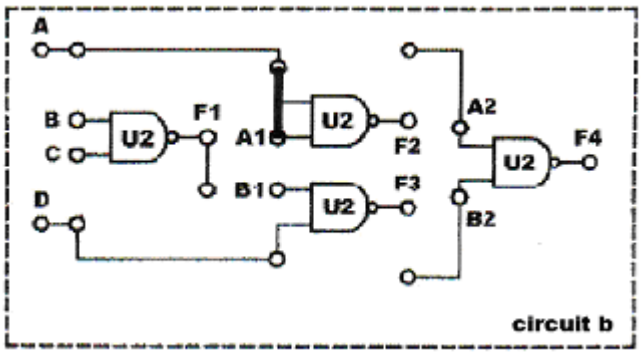
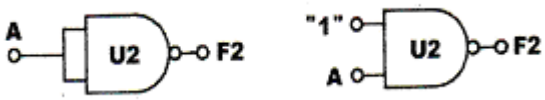


Fig. 2-5 (a)



(b) NOT gate constructed with NAND gate

(1) Connect input A to Data Switch SW1 and output F2 to A2 and Logic Indicator L1; connect 131 to Vcc ("1 "). Observe the output states.
When SW1="0", F2= _____
When SW1="1 ", F2= _____
Does the circuit act as a NOT gate?
(2) Connect input A1 to Vcc ("1 ") and remove the connection clip between A and A1 to create the NOT gate shown on the right side of Fig. 2-5 (b). Other connections remain the same. Observe the output states.

When SW1="0", F2= _____
When SW1="1", F2= _____
Does the circuit act as a NOT gate?

(3) Remove connection clips and insert them again according to Fig. 2-6 (a) to construct the AND gate shown in Fig. 2-6 (b). Connect A to SW1, A1 to SW2 and F4 to L1. Follow the input sequences given below and record the outputs in Table 2-4.

Does the circuit act as an AND gate (F=AxB)?

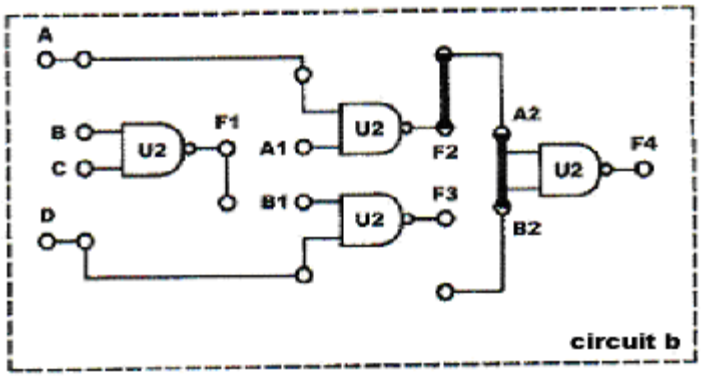


Fig. 2-6 (a)

Table 2-4

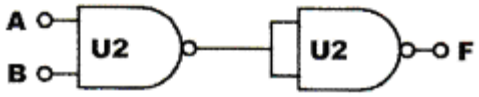


Fig. 2-6 (b)

2. Insert connection clips according to Fig. 2-7 (a) to construct the circuit of Fig. 2-7 (b). Connect A to A1 and SW1; F2 to A2; D to 131 and SW2; F3 to 132; F to 1-1. Follow the input sequences in Table 2-5 and record the outputs.

Does the circuit act as an OR gate (F=A+B)?

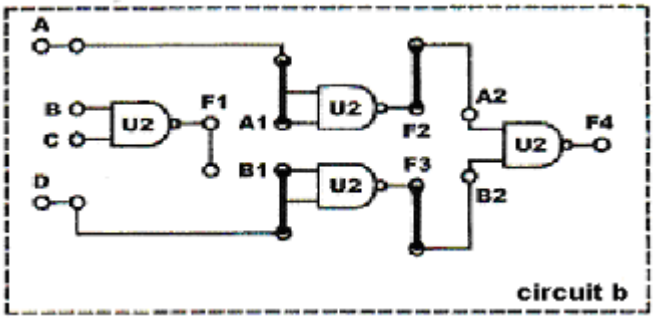
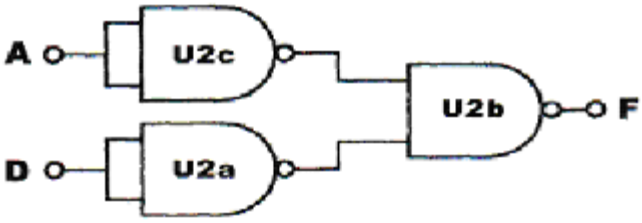


Fig 2.7 (a)



(b) OR gate constructed with NAND gate

Table 2-5

RESULTS

1. NAND gates can be used to construct any basic logic gate.

2. There are two ways to construct inverters with NAND gates. Since the high state of TTL consumes almost no current, if NAND gates are used to construct inverters the spare input should be connected to high potential.

FAULT SIMULATION

1. The output F2 remains in low state when U2b is used to construct a NOT gate. What could be the faults?

2. When U2b, U2c, U2d are used to construct an OR gate, the output F remains in high state. What could be the faults?

Experiment 4 XOR Gate Circuit

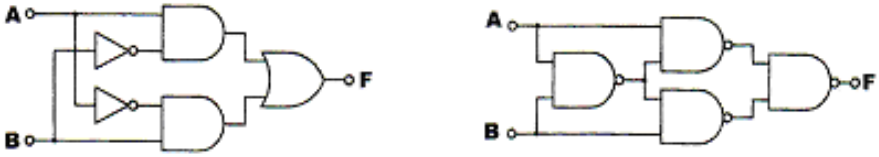
OBJECTIVE

Understand the characteristics of XOR gates.

DISCUSSION

The symbol of a XOR gate is shown in Fig. 2-8. The output F is equal to $\overline{A \oplus B} = \bar{A}B + A\bar{B}$. XOR gates can be constructed using NOT, OR, AND, NOR or NAND gates or by using four NAND gates, as shown in Fig. 2-9 (a) and (b).

Fig. 2-8 Symbol of XOR gate



(a) with basic gates (b) with NAND gates only

Fig. 2-9 XOR gate circuits

Since F= $\bar{A}B+A\bar{B}$, when B=0 F= $\bar{A}$ x 0+Ax 0=Ax1=1 and the circuit act as buffer. When B=1, F = $\bar{A}$ x 1 + A x $\bar{1}$ = $\bar{A}$ x 1= $\bar{A}$, the circuit act as an inverter. In other words, the input state of a XOR gate determines whether it will act as a buffer or an inverter. In this experiment, we will use basic logic gates to construct XOR gates and study the relationship between the inputs and outputs.

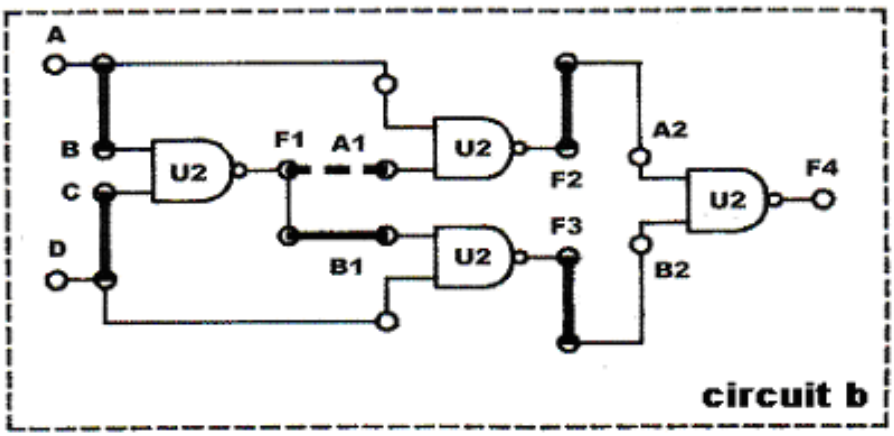
EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, DLLT-EM02: Assembled Logic Circuits (1) Experiment Module

EXERCISE

(a) Constructing XOR gate with NAND gate (Module DLLT-EM02 circuit b)

1. Insert connection clips according to Fig. 2-10 (a) to construct the circuit of Fig. 2-10 (b). Connect inputs A to SW1, D to SW2; outputs F1 to L1, F2 to L2; F3 to L3 and F4 to L4.



UT	OUTPUT

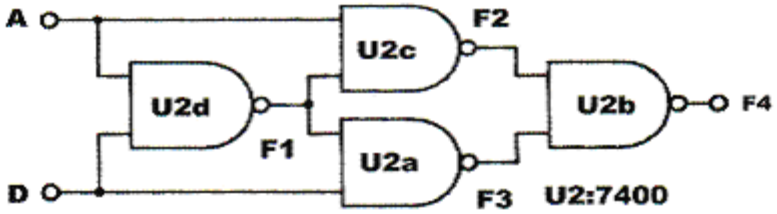


Fig 2.10 (a)

Fig 2.10 (b) equivalent circuits

2. Follow the input sequences for A and D in Table 2-6 and record the outputs.

INPUT)	OUTPUT

3. Determine the Boolean expression for F1, F2, F3, F4.

(b) Constructing XOR Gate with Basic Gate (DLLT-EM02 circuit c)

1. Insert connection clips according to Fig. 2-11 (a) to construct the equivalent circuit of Fig. 2-11(b).

2. Connect input A, B to SW1 SW2; outputs F1, F2, F3, to L1, L2, L3.

3. Follow the input sequences for A and B in Table 2-7 and record the output.

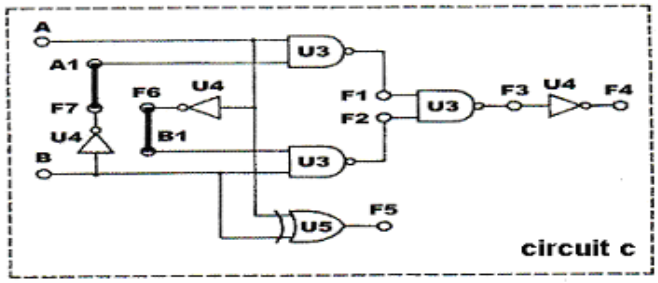


Fig 2.11 (a)

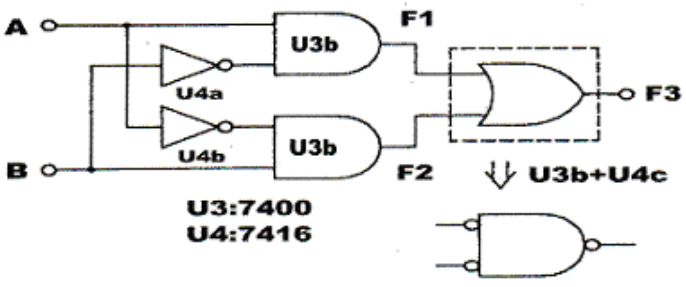


Fig 2.11 (b) equivalent circuits

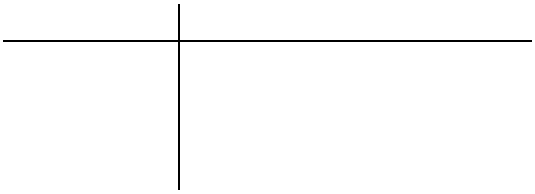


Table 2-7

1. Can this work as an XOR gate? If not how to modify it?

RESULTS

1. XOR gate can be constructed with either basic gates or four NAND gates with the same results. However, using four NAND gates is much simpler.

2. By adding a NOT gate to the output of a XOR gate it can be converted into an XNOR.

FAULT SIMULATIONS

1. What could be wrong if 4 NAND gates are used to construct a XOR gate and the output F=D?

2. What could cause the output F3 of a XOR gate made with basic gates to remain in high state?

Experiment 5: FLIP-FLOPS

OBJECTIVES:

• Construct and investigate the operation of various types of Flip-Flops.

Equipment and ICs:

• Lab. kit
• IC 7400 Quad NAND gates
• IC 7402 Quad NOR gates
• IC 7476 Dual J K-type flip-flops
• IC 7474 Dual D-type flip-flops

Introduction:

In digital circuits, a flip-flop is a term referring to an electronic circuit that has two stable states and thereby is capable of storing one bit of binary information and therefore, can serve as one bit of memory.

The major differences among various types of Flip-Flops are in the number of inputs they possess and in the manner in which they affect the binary state.

We will examine the:

- Basic Flip-Flop.
- SR Flip-Flop.
- D Flip-Flop.
- JK Flip-Flop.
- T Flip-Flop.

1.1 Basic and SR Flip-Flops

Basic Flip-Flop:

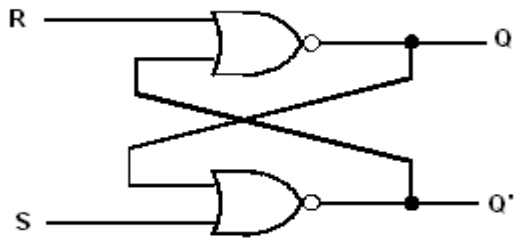


Figure 1

The Basic flip-flop operation is as follows (there is no clock):

1. S=0, R=0: No Change. Q will not change state (neither will Q')
2. S=0, R=1: Reset. Q gets reset (goes to 0). Q will be a 1.
3. S=1, R=0: Set. Q gets set (goes to 1). Q' will be a 0.
4. S=1, R=1: Not allowed.

SR Flip-Flop:

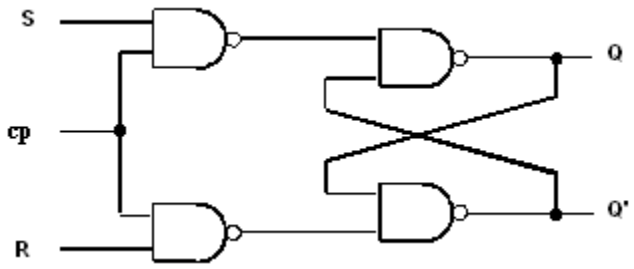


Figure 2

Lab Work:

1. Implement the circuit in Figure 1 on the kit using IC 7402 which has four NOR gates. (Note: there is no clock pulse)

a. Connect input S and R to a DIP switches.
d. Connect Q outputs of the flip-flop to two LEDs.

2. Set S to 0 and R to 1. This resets the flip-flop which means that Q is a 0 and Q' is a 1. This will always be the case when S=0 and R=1 regardless of the previous state of Q.
3. Go from S=0 and R=1 to S=0 and R=0. Q stays at 0 because SR=00 is the no change input combination and the previous state of Q was a 0.
4. Set S to 1 and R to 0. This input combination sets the flip-flop (Q=1, Q'=0) regardless of the previous state of Q.
5. Go from SR=10 to SR=00. This time Q stays at 1 which confirms that Q does not change state if S and R are 00.
6. Set S to a 1 and R to a 1. This input combination is disallowed since Q and Q' are both 0 and are not complements of each other. This input combination should always be avoided.
7. Do steps 2 through 5 a few more times to get the feel of the operation of the SR flip-flop. Include changing S and R from 01 to 10 and from 10 to 01.
8. Tabulate your observation in the characteristic table:

9. Connect the circuit shown in Figure 2. Notice that this implementation is different from the previous one in that S feeds into the gate whose output is Q and R feeds into the gate whose output is Q'. (Note: There is Clock pulse)

10. When Enable=1 enables the S and R inputs. To see what this means, set enable high and verify that the circuit works exactly like the circuit of Figure 2.

11. When Enable=0 disables the inputs. Show this by setting enable low and changing the S and R inputs. Notice that the outputs will not change regardless of what changes occur at S and R.

10. Repeat steps 2 through 7 to verify that this implementation of the SR flip-flop is equivalent to the Basic flip-flop.

Experiment 6
D Flip-Flop

D Flip-Flop:

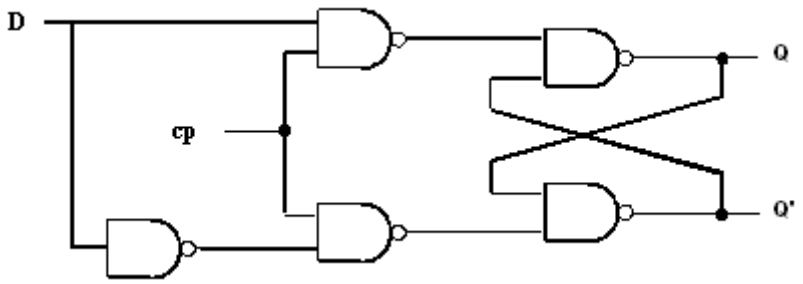


Figure 3

Lab Work:

1. Implement the circuit in Figure 3 on the kit using two of IC 7400 which has four NAND gates.

a. Connect input D to a DIP switches.

d. Connect Q outputs of the flip-flop to two LEDs.

2. With the D input remaining low, change the clock from low to high. Notice that the state of Q has changed from 1 to 0. Q' has also changed.

3. Change the D input to a 1 and change the clock from a 1 to a 0. Notice that the state of Q did not change to the input present at the D input since the proper clock transition was not provided. Change the clock back to a 1 and notice that Q changes to a 1.

4. Practice making Q a 1 and a 0 by changing the state of the D input and toggling the clock.

5. Tabulate your observation in the characteristic table:

D	Q	'

Experiment 7 JK Flip-Flop

JK Flip-Flop:

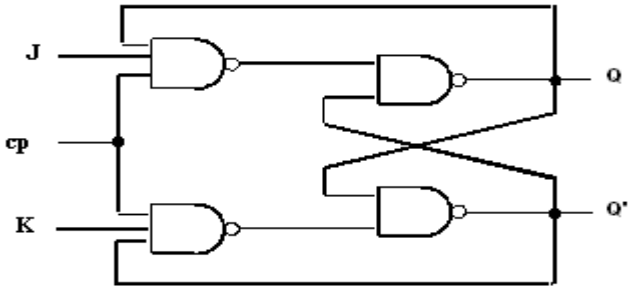


Figure 4

The JK flip-flop operation is as follows:

a. J=0, K=0: No Change. Q will not change state (neither will Q') when a negative edge is supplied to the clock.

b. J=0, K=1: Go to 0. Q will become a 0 (Q' goes to 1) when a negative edge is supplied to the clock.

c. J=1, K=0: Go to 1. Q will become a 1 (Q' goes to 0) when a negative edge is supplied to the clock.

d. J=1, K=1: Complement. Q gets the complement of its previous state (as does Q') when a negative edge is supplied to the clock.

Lab Work:

1. Implement the circuit in Figure 3 on the kit using two of IC 7400 which has four NAND gates.

   a. Connect input J and to a DIP switches.

   d. Connect Q outputs of the flip-flop to two LEDs.

2. Construct a truth table similar to the one which was made for the D flip-flop. Include columns for J, K, Q, and Q'. Have the instructor check your characteristic table.

Experiment 8
DESIGN OF SEQUENTIAL CIRCUITS

OBJECTIVES:

- Design and implement sequential circuits

Equipment and ICs:

- 2 - IC 7476 Dual J K-type flip-flops
- 2 - IC 7474 Dual D-type flip-flops
- 2 – IC 7400 Quad NAND gates

Introduction:

A sequential circuit is made up of flip-flops and combinational gates. The design of the circuit consists of choosing the flip-flops and then finding a combinational gate structure that, together with the flip-flops, produces a circuit that fulfills the stated specifications.

The number of flip-flops is determined from the number of states needed in the circuit. The combinational circuit is derived from the state table by evaluating the flip-flop input equations and output equations.

The procedure for designing synchronous sequential circuits can be summarized by a list of recommended steps:

1. Derive a state diagram from given specifications.
2. Obtain a state table from given specifications or state diagram.
3. Reduce the number of states if necessary.
4. Choose the type of flip-flops to be used.
5. Derive the simplified flip-flop input equations and output equations.
6. Draw the logic diagram.

An example for implementing a sequential circuit whose state diagram is given is shown in the Figure 1 below.

Present state					Ou	Flip-flop inpu			

Figure 1: state diagram and the state table of the sequential circuit.

Since there are 4 states, two Flip-flops will be required to implement the circuit Flip-flop inputs for a D Flip-flop are same as the Next State values and the output equation is as follows:

$DA = A\,(t+1) = Ax + Bx$

$DB = B\,(t+1) = Ax + B'x$

$Y = AB$

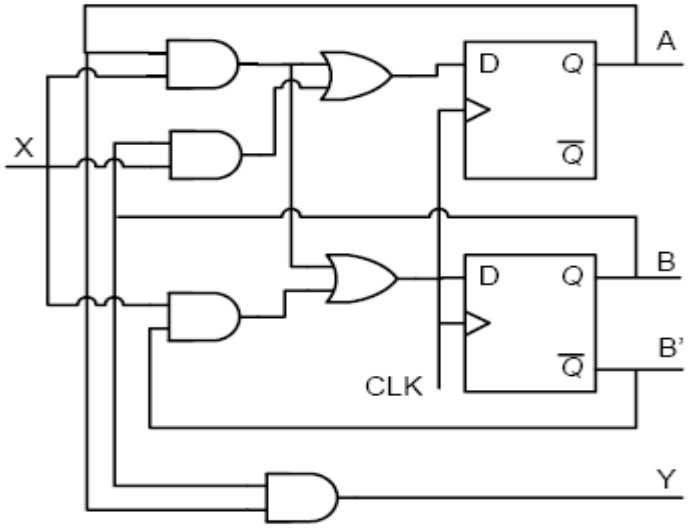


Figure 2: Implementation using D Flip-flops.

And the Flip-flop inputs for J K Flip-flop are:

JA = Bx KA = x'

JB = x KB = x' + A'

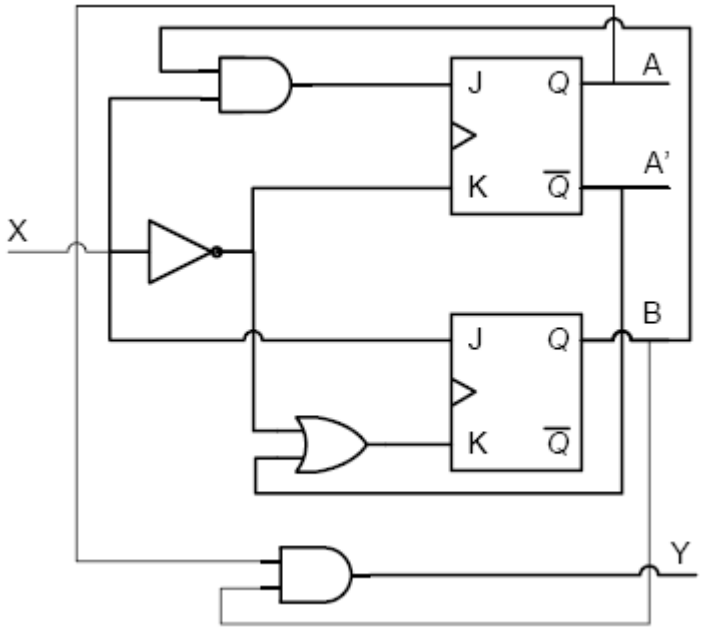
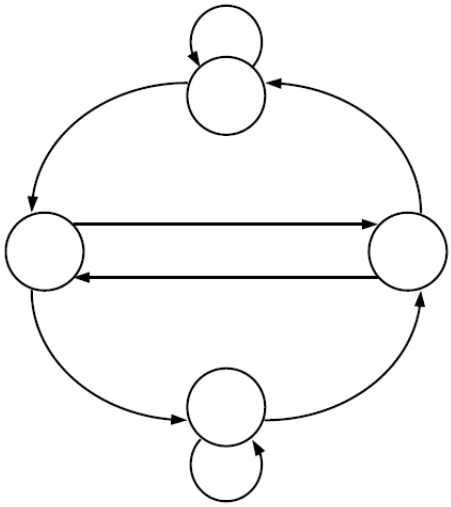


Figure 3: Implementation using J K Flip-flops.

2.1 Sequential Circuit Design

Design a sequential circuit using JK flip-flops whose state diagram is shown in Figure 2 below. Designate the two flip-flops as A and B, the input as X, and the output as Y.



Pre-lab Work:

1. Obtain the state table from the state diagram.

2. Obtain simplified flip-flop input equations and output equation.

_____

_____

_____

3. Draw the logic diagram of the circuit.

Lab Work:

1. Implement the sequential circuit (you designed in the pre-lab) on the breadboard using IC 7476 which has two JK-type Flip-flops and any external gates required.

a. Connect input X to a DIP switch.
b. Connect PRESET and CLEAR inputs to logic-1.
c. Connect CLK input to a pulser-button.
d. Connect Q outputs of flip-flops A and B to two LEDs.

2. Apply clock pulses to the circuit by pushing the pulser-button and verify the state transition and output as shown in Figure 2 above.

3. Now connect the output of flip-flop B to the input X and observe the sequence of states and output that will occur with the application of clock pulses. Tabulate your observations in the form of a state table or draw a state diagram.

4. Record your results and observations for the lab report.

2.2 Counter Design

Design a counter that goes through the following sequence of binary states: 0, 1, 2, 3, 6, 7, 10, 11, 12, 13, 14, 15, and back to 0 to repeat. Note that binary states 4, 5, 8, and 9 are not used. The counter must be self-starting; that is, if the circuit starts from any one of the four invalid states, the count (clock) pulses must transfer the circuit to one of the valid states to continue to count correctly. Use J K flip-flops for your design.

Pre-lab Work:

1.Draw the state diagram for the counter.

2. Derive the state table from the state diagram.

3. Obtain simplified flip-flop input equations.

_____

_____

_____

4. Draw the logic diagram for the counter circuit.

Lab Work:

1. Implement the sequential circuit (you designed in the pre-lab) on the breadboard using IC 7476 which has two J K-type Flip-flops and any external gates required.

a. Connect PRESET and CLEAR inputs to logic-1.
b. Connect CLK input to a pulser-button.
c. Connect Q outputs of all flip-flops to LEDs.

2. Apply clock pulses to the circuit by pushing the pulser-button and verify the required count sequence.

3. Verify that the circuit is self-starting by initializing the circuit to each unused state by means of the PRESET and CLEAR inputs and then applying pulses to see whether the counter reaches one of the valid states.

4. Record your results and observations for the lab report.

Experiment 9
Command Reference

We introduce here some of the commands that will be studied in the course:

Command	Description
`Cat`	Joins and displays files
`Cmp`	Compares two files
`Cp`	Copies files
`Find`	Finds files based on criteria
`gzip`	Compresses or decompresses files
`head`	Displays the beginning of a file
`less`	Displays text files, one screen at a time
`ls`	Displays information about one or more files
`man`	Displays documentation for commands
`mkdir`	Creates a directory
`mv`	Renames or moves a file
`rm`	Removes a file (deletes a link)
`rmdir`	Removes a directory
`tail`	Displays the last part (tail) of a file
`cd`	Changes to another working directory
`chgrp`	Changes the group associated with a file
`chmod`	Changes the access mode (permissions) of a file
`chown`	Changes the owner of a file and/or the group the file is associated with
`date`	Displays or sets the system time and date
`kill`	Terminates a process by PID
`ps`	Displays process status
`which`	Shows where in PATH a command is located
`who`	Displays information about logged-in users

Digital Logic Design Laboratory Experiment 1 MultiSIM

This experiment is designed to give the students some experience with the laboratory equipment and software tools. It will not be graded and a lab report is not necessary.

Objective: To get familiarized with MultiSIM.

Required Equipment: The MultiSIM software.

Laboratory Procedure:

Locate the MultiSIM software on the laboratory computers.

Enter a circuit into MultiSIM which implements the function D=A·B+C using a 2-input AND gate, a 2-input OR gate, and an LED. This will appear as an AND gate with two switches labeled A and B as inputs, an OR gate with one switch labeled C as one input and another from the output of the AND gate, and an LED labeled D as output. Test your circuit by checking the output D for every combination of A, B and C. Doing so should produce the truth table of the circuit.

Repeat step 2 with the circuit for Z=W·(X+Y).

Enter a new circuit into MultiSIM which implements the function E=A·B+C·D using standard 74LS series components rather than logic gates. Generate the truth table and timing diagram of output versus inputs.

Repeat step 4 with the circuit for Q=(A·B)+(A'·C·D)+(B'·D').

Repeat step 4 with the circuit for P=(A+B)·(A'+C+D)·(B'+D').

Experiment 2

Logic Design Using NOR and NOT Gates

Objective: To review Boolean and combinational logic. To implement and test combinational logic circuits using MultiSIM. Also, to build and test the circuit using 74LS series chips.

Required Equipment: The MultiSIM software, 74LS02, 74LS27 and 74LS04 logic gates, one switch/LED box, 5V power supply, breadboard and wires.

- Preparatory Exercises: Use the TTL data sheets available on the class web-site to answer the following questions.

What is the typical propagation delay in nanoseconds for the 74LS02, 74LS27 and 74LS04 logic gates?

What is the maximum propagation delay in nanoseconds for the 74LS02, 74LS27 and 74LS04 logic gates?

Use minimal multilevel logic design and 2-input, 3-input NOR gates and inverter gates only to design the following:

$$F(A, B, C, D) = \mathbf{\Pi M}((2, 4, 5, 6, 8, 10, 12, 13) \cdot \mathbf{\Pi D}(0, 11)$$

1) Laboratory Procedure: a) Simulate the designs of Preparatory Exercises 3 with MultiSIM using the appropriate 74LS series chips. b) Develop truth tables and timing diagram for output versus inputs. c) Indicate the worst-case delay situation and worst-case delay time calculation. d) Connect the circuit that you designed and simulated on the breadboard using the 74LS series chips. Use the switch/LED box to confirm proper operation of the circuit. Show this to your lab instructor.

2) Report contents:

1 A title page (including course name, experiment number and name, instructor's name, group number, student names, and date)

2 Answers of the above preparatory exercises.

3 A description of the design process in sufficient detail for a reader without the assignment sheet to be able to follow the design from inception to completion, i.e., K-maps and minimized equations.

4 Circuit diagrams, truth tables, timing diagrams, and delay calculations.

5 Comments on the experiment including any difficulties encountered.

- Report Preparation: All material included should be presented in neat and orderly fashion. Use of a word processor and drawing package is required.

Experiment 3

Logic Design Using NAND and NOT Gates

Objective: To review Boolean and combinational logic. To implement and test combinational logic circuits using MultiSIM. Also, to build and test the circuit using 74LS series chips.

Required Equipment: The MultiSIM software, 74LS00, 74LS10 and 74LS04 logic gates, one switch/LED box, 5V power supply, breadboard and wires.

- Preparatory Exercises: Use the TTL data sheets available on the class web-site to answer the following questions.

  What is the typical propagation delay in nanoseconds for the 74LS00, 74LS10 and 74LS04 logic gates?

  What is the maximum propagation delay in nanoseconds for the 74LS00, 74LS10 and 74LS04 logic gates?

  Use minimal multilevel logic design and 2-input and 3-input NAND gates and inverter gates only to design the following:

$$F(a, b, c, d) = \Sigma m(0, 1, 3, 4,6, 7, 8,10,11,15) + \Sigma d(5, 9)$$

3) Laboratory Procedure: a) Simulate the designs of Preparatory Exercises 3 with MultiSIM using the appropriate 74LS series chips. b) Develop truth tables and timing diagram for output versus inputs. c) Indicate the worst-case delay situation and worst-case delay time calculation. d) Connect the circuit that you designed and simulated on the breadboard using the 74LS series chips. Use the switch/LED box to confirm proper operation of the circuit. Show this to your lab instructor.

4) Report contents:

1 A title page (including course name, experiment number and name, instructor's name, group number, student names, and date)

2 Answers of the above preparatory exercises.

3 A description of the design process in sufficient detail for a reader without the assignment sheet to be able to follow the design from inception to completion, i.e., K-maps and minimized equations.

4 Circuit diagrams, truth tables, timing diagrams, and delay calculations.

5 Comments on the experiment including any difficulties encountered.

- Report Preparation: All material included should be presented in neat and orderly fashion. Use of a word processor and drawing package is required.

Experiment 4

Combinational Logic Design

Objective: To design a minimal cost multiple-output combinational logic network using commercially available inverters and NAND gates.

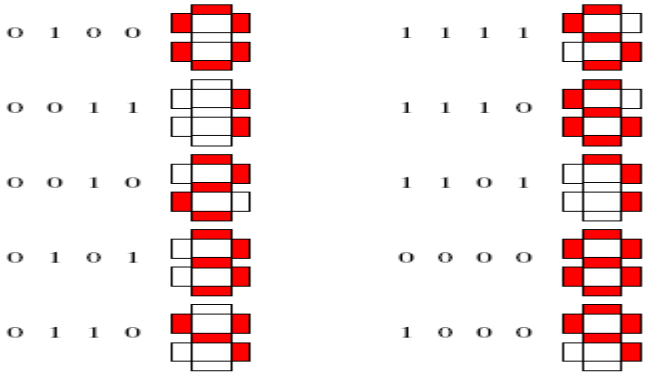
Required Equipment: The MultiSIM software, one switch/LED box, 5V power supply, prototyping board, 74LS00, 74LS04, and 74LS10 logic gates, a 74LS47 BCD to 7-segment decoder, 7-segment LED display, a logic probe and a digital pulser.

- Preparatory Exercises

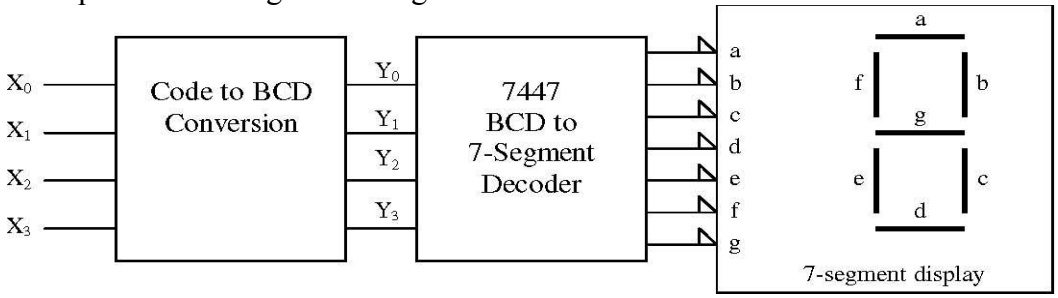
Review multiple-output design techniques. Use the TTL data sheets available on the class web-site to familiarize yourself with the 74LS series gates.

The 74LS47 BCD to 7-segment decoder will drive a 7-segment LED display to output the digits 0-9 in response to BCD encoded 4-bit input.

Using the following table of input/output relationships, design the combinational logic necessary to turn on the required segments of the seven-segment display for the indicated input vectors. Your logic will convert the four bit codes below into 4-bit BCD. Use only inverters, 2-input NAND, and 3-input NAND gates in your design. Assume that any input vectors, which are not listed, will never occur and may be treated as don't cares.

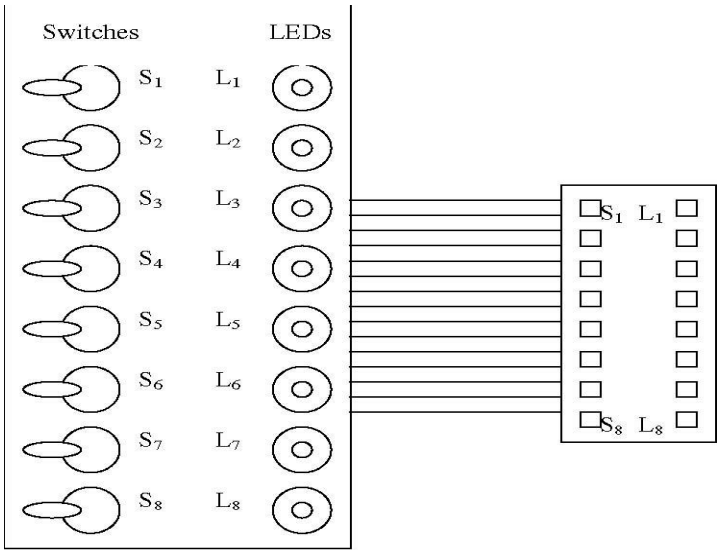


This is a 4-input, 4-output system and your design should make use of multiple-output techniques to reduce the necessary logic. Design for minimum chip count. You should not need more than five of the specified chips for this design including the 74LS47 decoder.



A data sheet is provided to describe the functionality of the 7-segment display.

The switch/LED box used for input and output is connected via a ribbon cable and DIP connector as shown in the following diagram. To use, apply 5V to the red terminal and Ground the black terminal, then connect the switches and LEDs as needed.



- Laboratory Procedure

1 Simulate your design with MultiSIM using 74LS00, 74LS04, 74LS10, and 74LS47 chips. Hand in printouts of your circuit design and a timing diagram showing all possible input combinations.

2 Connect the circuit you designed and simulated using MultiSIM on the prototyping board using the appropriate 74LS series chips. Use the switch/LED box to confirm proper operation of the circuit. Show this to your lab instructor.

3 Try the-don't care inputs. Do they operate as you expected from your circuit diagram?

4 Calculate the chip cost of your design.

5. Comments on the experiment including any difficulties encountered.

5) Report contents:

1 A title page (including course name, experiment number and name, instructor's name, group number, student names, and date)

2 Answers of the above preparatory exercises.

3 A description of the design process in sufficient detail for a reader without the assignment sheet to be able to follow the design from inception to completion, i.e., K-maps and minimized equations.

4 Circuit diagrams, truth tables, timing diagrams, and delay calculations.

- Report Preparation: All material included should be presented in neat and orderly fashion. Use of a word processor and drawing package is required.

Experiment 5

D Flip-Flop

Objectives: To build and utilize a D flip-flop circuit.

Required Equipment: The MultiSIM software, 74LS series chips, one switch/LED box, 5V power supply, breadboard and wires.

- Preparatory Exercises: Review the operation and uses for D flip-flops in your digital logic design texts. Also review the specifications for the 74LS74 IC in the TTL data sheets.

  Give a brief description of the use of D flip-flops in logic design.

  Develop a 74LS74 D flip-flop using 2-input and 3-input NAND gates. Simulate it using MultiSIM. Submit a clearly labeled circuit diagram.

  For the circuit developed in Exercise 2, calculate the worst-case propagation delay from positive edge of clock to outputs, and from reset and preset inputs to outputs. In addition, calculate the worst-case data setup time for input D relative to positive edge of clock.

  In the design above, beginning in each case from reset:What happen if D=1and a clock pulse occurs?What happen if D=0 and a clock pulse occurs?

  Connect the designed circuit using TTL NAND IC's and be prepared to operate the circuit using the switch/LED boxes during the lab.

- Laboratory Procedure:

  Simulate the circuit developed above with MultiSIM using NAND IC's.

  Using the circuit designed and assembled in the Preparatory Exercises, correct any design errors, and demonstrate the operation of the circuit.

  The switch/LED boxes will be available during the lab for debugging and demonstration purposes.

  The circuits should perform all the functions provided by the 74LS74 gates including the set and reset.

  Treat all incoming signals including the clock as inputs controlled by the switch box and both Q and Q' as outputs to the LEDs.

  Demonstrate proper operation of the circuit to the lab instructor.

- Report Contents:

  A title page (including course name, experiment number and name, instructor's name, group number, student names, and date)

  Answer of the above preparatory exercises.

  A description of the process in sufficient detail for a reader without the assignment sheet to be able to follow the design from inception to completion.

  A circuit diagram for the circuit and any requested tables, diagrams, and calculations.

  Comments on the experiment including any difficulties encountered.

- Report Preparation: All material included should be presented in neat and orderly fashion. Use of a word processor and drawing package is required.

Experiment 6
J-K Flip-Flop

Objectives: To build and utilize a J-K flip-flop circuit.

Required Equipment: The MultiSIM software, 74LS series chips, one switch/LED box, 5V power supply, breadboard and wires.

- Preparatory Exercises: Review the operation and uses for J-K flip-flops in your digital logic design texts. Also review the specifications for the 74LS76A IC in the TTL data sheets.

  Give a brief description of the uses of J-K flip-flops in logic design.

  Develop a 74LS76A J-K flip-flop using 2-input and 3-input NAND gates. Simulate it using MultiSIM. Submit a clearly labeled circuit diagram.

  For the circuit developed in Exercise 2, calculate the worst-case propagation delay from negative edge of clock to outputs, and from reset and preset inputs to outputs. In addition, calculate the worst-case data setup time for inputs J and K relative to negative edge of clock.

  In the design above, beginning in each case from reset:What happen if J=0, K=0 and a clock pulse occurs?What happen if J=0, K=1 and a clock pulse occurs?What happen if J=1, K=0 and a clock pulse occurs?What happen if J=1, K=1 and a clock pulse occurs?

  Connect the designed circuit using TTL NAND IC's and be prepared to operate the circuit using the switch/LED boxes during the lab.

- Laboratory Procedure:

  Simulate the circuit developed above with MultiSIM using NAND IC's.

  Using the circuit designed and assembled in the Preparatory Exercises, correct any design errors, and demonstrate the operation of the circuit.

  The switch/LED boxes will be available during the lab for debugging and demonstration purposes.

  The circuits should perform all the functions provided by the 74LS76A gates including the set and reset.

  Treat all incoming signals including the clock as inputs controlled by the switch box and both Q and Q' as outputs to the LEDs.

  Demonstrate proper operation of the circuit to the lab instructor.

- Report Contents:

  A title page (including course name, experiment number and name, instructor's name, group number, student names, and date)

  Answer of the above preparatory exercises.

  A description of the process in sufficient detail for a reader without the assignment sheet to be able to follow the design from inception to completion.

  4. A circuit diagram for the circuit and any requested tables, diagrams, and calculations.

  Comments on the experiment including any difficulties encountered.

- Report Preparation: All material included should be presented in neat and orderly fashion. Use of a word processor and drawing package is required.

Experiment 7: Shift Register Counters

Objective: To synthesize two shift register counters; a Johnson Counter and a Ring Counter from appropriate flip-flop circuits.

Required Equipment: The MultiSIM software. 74LS series chips, LED/Switch box, wire and breadboard.

Read sections in the TTL data sheets pertaining to the 74LS74 dual D flip-flop

- For a Johnson Counter:

1. Design a simple 4-bit Johnson Counter by using D flip-flops. The counter should count in the following order:

0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000, 1000……

What is the least number of flip-flops needed to design a 4-bit Johnson Counter? How many 74LS74 chips do you need?

Include in the design a means for resetting the counter to 0000.

Provide circuit diagrams, relevant truth tables, state diagrams and state tables.

- For a Ring Counter:

1. Design a simple 4-bit Ring Counter by using D flip-flops. The counter should count in the following order:

1000, 0100, 0010, 0001, 1000, 0100, 0010, 0001, 1000, 0100…..

What is the least number of flip-flops needed to design a 4-bit Ring Counter? How many 74LS74 chips do you need?

Include in the design a means for resetting the counter to 1000.

Provide circuit diagrams, relevant truth tables, state diagrams and state tables.

- Laboratory Procedure

Simulate the designed circuits above with MultiSIM using appropriate chips.

Connect both the Johnson Counter and the Ring Counter circuits designed in the preparatory exercise using the appropriate TTL IC chips. Arrange the breadboard so that it may be connected to a switch/LED box. You would have two input switches -RESET and CLOCK, and four output states shown by LED -Q_0, Q_1, Q_2, and Q_3.

Demonstrate the correct operation of your circuits to the lab instructor.

- Report Contents:

A Title Page (including course name, experiment number and name, instructor's name, student's name, group number, and date)

Answers of the above preparatory exercises.

A description of the design process in sufficient detail for a reader without the assignment sheet to be able to follow the design from inception to completion (state diagram, state transition table).

A correct list of the input functions to the flip-flops.

A circuit diagram for each circuit, timing diagrams, and any requested calculations.

Sample calculations of the worst-case delay in the excitation function circuits and a discussion of the impact of these delays on the maximum clock frequency of the counter.

Comments on the experiment including any difficulties encountered.

- Report Preparation: All material included should be presented in neat and orderly fashion. Use of a word processor and drawing package is required.

Digital Logic Design Laboratory

Experiment 8

Sequential Network Design Using J-K Flip-Flops

Objective: To design sequential networks using J-K flip-flops.

Required Equipment: The MultiSIM software. 74LS series chips, LED/Switch box, wire and breadboard.

- Preparatory Exercises

Read sections in the TTL data sheets pertaining to the 74LS76A Dual J-K flip-flop.

1 For the 74LS76A, what is the maximum clock rate, minimum pulse width for the clock's high and low levels, worst case propagation delay of the outputs from the high-to-low clock transition, and minimum input setup time?

2 Design a nine-step counter to count in the following sequence. Use J-K flip-flops, NAND gates, and Inverters only. 0011, 0101, 1001, 1000, 1011, 1010, 0110, 0100, 0111, 0011, … Include in the design a means for resetting the counter to 0011. Provide a circuit diagrams, relevant truth tables, state diagrams and state table. In addition, provide the excitation functions for the J-K flip-flops.

- Laboratory Procedure

1 Simulate the designed network above with MultiSIM using appropriate chips.

2 Connect the network designed in Preparatory Exercise 4, using the appropriate TTL integrated circuit chips. Arrange the breadboard so that it may be connected to a switch/LED box. The circuit input and output lines should match the following arrangement.

Switches		LEDS
Clock •	•	Q of J-K 3 (MSB)
Reset •	•	Q of J-K 2
	•	Q of J-K 1
	•	Q of J-K 0 (LSB)

3. Demonstrate the correct operation of your circuit to the lab instructor.

- Report Contents:

1 A Title Page (including course name, experiment number and name, instructor's name, student's name, group number, and date)

2 Answers of the above preparatory exercises.

3 A description of the design process in sufficient detail for a reader without the assignment sheet

to be able to follow the design from inception to completion (state diagram, state transition table, K-maps, and minimized equations).

4 A correct list of the input functions to the flip-flops.

5 A circuit diagram for the circuit, timing diagrams, and any requested calculations.

6 Sample calculations of the worst-case delay in the excitation function circuits and a discussion of the impact of these delays on the maximum clock frequency of the counter.

7 Comments on the experiment including any difficulties encountered.

- Report Preparation: All material included should be presented in neat and orderly fashion. Use of a word processor and drawing package is required.

Digital Logic Design Laboratory

Experiment 9

Sequential Network Design Using D Flip-FlopsSimple Vending Machine

Objective: To design sequential networks using D flip-flops.

Required Equipment: The MultiSIM software. 74LS series chips, LED/Switch box, wire and breadboard.

- Preparatory Exercises

1 For the 74LS74, what is the maximum clock rate, minimum pulse width for the clock's high and low levels, worst-case propagation delay of the outputs from the low-to-high clock transition, and minimum input setup time?

2. Design a clocked sequential network to accept two inputs and drive four outputs.

a. The two inputs are for a "nickel" and a "dime". Each input is a logic 1 when the respective coin is inserted.

b. The four outputs are four indicator lamps which indicate to the customer what to do: "Insert 10 cents", "Insert 5 cents", "Dispensing item", and "Giving change". Note that the outputs will be a function of the state of the system.

c. The "giving change" light is for the case where the customer inserts a nickel and then a dime.

d. Assume that the input signal for the coin is only high for one clock cycle per coin and that only one coin is inserted at a time.

e. The "give change" and "dispense item" output lights are only high for one clock cycle.

f. Once an item is dispensed, start over. (Return to the "insert 10 cents" state.)

Example:

```
N               : 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0
D               : 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0
Insert 10 cents: 1 1 0 0 0 0 0 1 1 1 0 1 1 1 0 0 0 0 1 1
Insert 5 cents : 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0
Giving change  : 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Dispensing item: 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 1 0 0
```

1 Your circuit should include an active low signal for manually resetting the flip-flops to a "start" state ("Insert 10 cents"). The minimum solution for this implementation requires four states.

2 The design may include NAND gates, Inverters, NOR gates, and exactly two D flip-flops.

3 Note that you will need to design both a state machine, in which the next state is a function of the current state and the inputs, and an output network, in which the four outputs are a function of the current state.

6. For the preparatory exercises, the circuit is to be simulated using MultiSIM and the following must be turned in:

a. A circuit diagram clearly indicating chip connections.
b. A timing diagram that shows the correct behavior given three scenarios:
i. Insert nickel and then dime
ii. Insert dime
iii. Insert two nickels
c. Calculation of three parameters

i. The fastest possible clock frequency
ii. The minimum setup time for the inputs "Nickel" and "Dime"
iii. The maximum delay from the clock to output indicators valid

- Laboratory Procedure
  1 Simulate the designed network above with MultiSIM using appropriate chips.
  2 Connect the network designed above using the appropriate TTL integrated circuit chips. Arrange the breadboard so that it may be connected to a switch/LED box. The circuit input and output lines should match the following arrangement.

  Switches LEDSReset ••Q of D1 (MSB)Clock ••Q of D2 (LSB)Dime ••Insert 10 centsNickel ••Insert 5 cents
  ••Dispense item ••Give change

3. Demonstrate the correct operation of your circuit to the lab instructor.

- Report Contents:
  1 A Title Page (including course name, experiment number and name, instructor's name, student's name, group number, and date)
  2 Answers of the above preparatory exercises.
  3 A description of the design process in sufficient detail for a reader without the assignment sheet to be able to follow the design from inception to completion (state diagram, state transition table, K-maps, and minimized equations).
  4 A correct list of the input functions to the flip-flops.
  5 A circuit diagram for the circuit, timing diagrams, and any requested calculations.
  6 Sample calculations of the worst-case delay in the excitation function circuits and a discussion of the impact of these delays on the maximum clock frequency of the counter.
  7 Comments on the experiment including any difficulties encountered.

- Report Preparation: All material included should be presented in neat and orderly fashion. Use of a word processor and drawing package is required.

Digital Logic Design Laboratory

Experiment 10

Six-Sided Electronic Dice Roller

Objective: To use both sequential and combinational logic circuits to build a "real world" application -an Electronic Dice Roller.

Required Equipment: The MultiSIM software, 74LS series chips, 7-segment display, wire and breadboard, and LED/Switch box.

•Preparatory Exercises Review TTL data sheets of 74LS76A, 74LS47, 74LS00 and 74LS04. Also, review the pin connection for 7-segment display.

1 First, design a counter using 74LS76A that counts repeatedly from 1 to 6. Each number must appear with the same frequency because a fair die is desired. You can use a down counter or up counter, as long as each number comes up as often as the others.

2 When RESET, the output is 1 for an up counter or 6 for a down counter.

3. You need a clock signal that cycles through the numbers quickly so that it is impossible for a human to control what number comes up. Hence, the number is, for all practical purpose, RANDOM. In order to make the clock signal cycles rapidly, you need an oscillator. You can build an inexpensive oscillator with the following circuit:

What does the oscillator do when N is an odd number?

What happens if N is an even number?

If you want a high speed oscillator, do you increase the number of N or do you decrease it?

3 The output is fed to the combination of a 74LS47 IC and a 7-segment display.

Laboratory Procedure:

Simulate you design with MultiSIM using appropriate chips. Are switches working better than the word generator for feeding in the inputs during simulation? Explain.

2. Connect the circuit you designed and simulated using MultiSIM on the prototyping board using appropriate 74LS series chips. Use switch/LED box

to confirm proper operation of the circuit. Show this to your lab instructor. Do they operate as you expected from your circuit diagram?

Do you or don't you see a dim "8" when the "Enable" switch of the oscillator is thrown ON? Explain.

Comment on the experiment including any difficulties encountered.

Calculate the total cost of your design.

- Report Contents:

A Title Page (including course name, experiment number and name, instructor's name, student's name, group number, and date)

Answers of the above preparatory exercises.

A description of the design process in sufficient detail for a reader without the assignment sheet to be able to follow the design from inception to completion (state diagram, state transition table, K-maps, and minimized equations).

A correct list of the input functions to the flip-flops.
A circuit diagram for the circuit, timing diagrams, and any requested calculations.
Sample calculations of the worst-case delay in the excitation function circuits and a discussion of the impact of these delays on the maximum clock frequency of the counter.
Comments on the experiment including any difficulties encountered.

- Report Preparation: All material included should be presented in neat and orderly fashion. Use of a word processor and drawing package is required.