Lab

C1114

كليه الهندسة - جامعة المنصورة

معمل الدوائر المنطقية C1114

Computers and Control Systems Engineering Department

قسم هندسة الحاسبات ونظم التحكم

Laboratory Book

Computers and Control Systems Engineering Department

2021

C1114 معمل الدوائر المنطقية

Laboratory Book

Part

1

1: Laboratory Basic Information

أولا : البيانات الأساسية للمعمل

اسم المعمل	الدوائر المنطقية
القسم العلمي	هندسة الحاسبات ونظم التحكم
المشرف	د/ نهى صقر د/نهلة بشرى
أمين المعمل	أ/ وليد أحمد على
الهيئة المعاونة	م/ إيمان عطية م/ آيه حمدى م/ نهى المنباوى
التليفون	داخلى 1492
الموقع بالنسبة للكلية	الناحية البحرية
مساحة المعمل	120متر^2

Part

2

2: Laboratory Instruments

ثانياً: قائمة بالأجهزة والمعدات الموجودة بالمعمل:

Serial Number	العدد	اسم الجهاز	م
	2	Digital Logic Lab trainer	1
	7	Assembled Logic circuits Experiment Module	2
	8	Converter circuits Experiment module	3
	2	Clock generator circuits Experiment module	4
	1	Sequential logic circuits Experiment module	5
	3	Memory circuits`	6
	2	Basic logic gates Experiment module	7
	3	Assembled logic circuits	8
MB ECS-G41 T.M	23	CPU Intel Core 2 Due 2/2.9M	9
MB Intel P.IV GB 945 chipset	1	CPU Intel P.IV 3 GHz	10

DLLT-EM01 : BASIC LOGIC GATE EXPERIMENTS

1-1 Introduction to Logics and Switches

1-2 Logic Gates Circuits

a. Diode Logic (DL) Circuit
b. Resistor-Transistor Logic (RTL) Circuit
c. Diode-Transistor Logic (DTL) Circuit
d. Transistor-Transistor Logic (TTL) Circuit
e. Complementary-Metal-Oxide-Semiconductor (CMOS) Circuit

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a. TTL Threshold Voltage Measurement
b. CMOS Threshold Voltage Measurement

1-4 Voltage/Current Measurement

a. TTL I/O Voltage and Current Measurement
b. CMOS Voltage and Current Measurement

1-5 Basic Logic Gate Transmission Delay Measurement

a. TTL Gate Delay Time Measurement
b. CMOS Gate Delay Time Measurement

1-6 Measurements of Basic Logic Gates Characteristics

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d. NAND Gate Characteristics Measurement
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1-7 Interfaces Between Logic Gates

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BASIC LOGIC GATE EXPERIMENTS

1-1 Introduction to logic and switches

OBJECTIVES `

1. Understanding how digital and analog signals function.
2. Understanding the relationship between switch and logic.

DISCUSSIONS

There are two types of matters, which occurs every moment in our daily life: The continuous or "Analog" matters and the non-continuous or "Digital" matters. Both matters will be discussed in this chapter.

Analog System

In the analog system, a mathematical quantity is expressed by a certain number or value directly proportional to it. For example, the odometer in a car will continuously indicate the speed by rotating the hand for a certain degree. As the speed or "input" changes, position of the hand or "output" will change as well, matching the current speed of the car. Both input and output are continuously changing. In fact, the analog system is actually a "Continuously Variable Presentation".

Digital System

In the digital system, quantities are expressed by segmented numbers or symbols rather than continuous proportional values. For example, a digital watch displays seconds, minutes, hours and dates in segments of one second. There are no continuous changes between one and two second when in fact there are indefinite divisions between one and two. On a digital watch, it is either "1" or "2" with nothing in between. You might say that digital watches with stopwatch function can count to one hundredth of a second but the fact remains that there are indefinite divisions between 0.001 and 0.002 seconds.

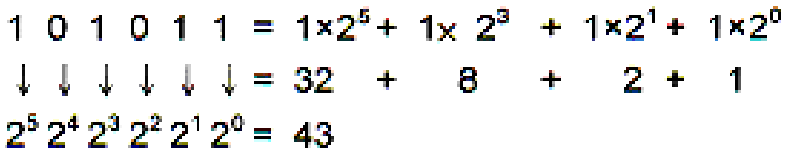
Since it is impossible to use indefinite digits to express a precise value, often an approximate number is used. For example, the circumference factor "π" lies somewhere between 3.14159 and 3.1416. Even with today advance technologies no one knows exactly what the precise value is. We usually assume it to be 3.1416, with four decimal points. In digital systems changes and outputs occur in predetermined segments with nothing in between. This is sometimes called "Non-continuous Changes".

Analog and digital system each has its own advantages. The analog system is easily calibrated, inexpensive, fast and accurate while the digital system is not easily influenced by physical conditions or material characteristic differences.

To combine the advantages each system offers, we can use the "Analog-Digital Converter" or "Digital-Analog Converter". But before doing so it is essential that we understand the various digital "systems".

Usually the decimal system, which uses numbers 0, 1,2,3,4,5,6,7, 8, 9 to represent all quantities with the largest number being 9, is used most often.

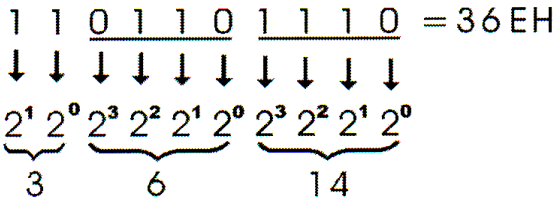
In the binary system only two states 0 and 1 exists. Following is an example on how to convert a binary number into a decimal number.



To make the conversion between decimal and binary systems easier, the octodecimal system was invented. The largest number in octodecimal system is 7, which is equivalent to binary 111.

To convert from binary to octodecimal, divide the binary number in groups of three starting from the left hand side. For example, the binary number 1010101 is equal to octodecimal 255.
In computers the hexadecimal systems are used. The largest hexadecimal number is 15 and in decimal 9, so the numbers used in hexadecimal system are 0, 1, 2 ...9, A, B, C, D, E, F

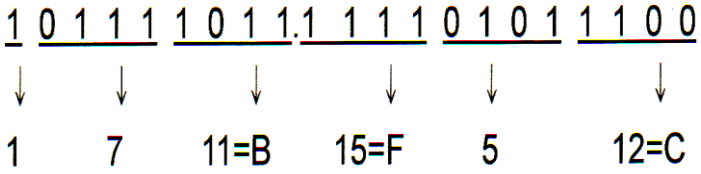
Since $16 = 2^4$ to convert binary numbers to hexadecimal numbers simple divide the binary number in groups of four starting from the left hand side. For example:



Of the binary, octodecimal and hexadecimal systems, the octodecimal system is the least used. Binary numbers are marked at the end with the letter "B", while hexadecimal numbers are marked with letter H.

Conversion between binary and hexadecimal numbers:
101111011.1111010111 = 17B.F5CH

Using the decimal point as the center, divide the binary number to the left in groups of four. Use the same procedure for the binary number to the right of the decimal point, adding a "0" at the end and we have:



To convert from decimal to binary, we can first convert decimal to octodecimal. For Example, convert decimal 86 to octodecimal:

$$
\begin{array}{r|l}
8 & 8\ 6 \\
\cline{2-2}
8 & 1\ 0 \\
\cline{2-2}
 & 1
\end{array}
$$

the remainder is 6 so 8^0 is 6

the remainder is 2 so 8^1 is 2

8^2 is 1

so $8\ 6_{10} = 126_8$

126_8 = 001010110B (B : Binary)

Example 2: Converting decimal 12.65 to binary

In this case, where demonical points are involved, we have to divide the conversion in two steps.

Decimal points: Multiply the decimal point by 8 as shown below. The whole numbers generated are the octodecimal numbers.

$$
\begin{array}{rl}
 & 0.65 \\
 & \times\ \ 8 \\
\hline
8^{-1} & \boxed{5}.20 \\
 & \times\ \ 8 \\
\hline
8^{-2} & \boxed{1}.6 \\
 & \times\ \ 8 \\
\hline
8^{-3} & \boxed{4}.8 \\
 & \times\ \ 8 \\
\hline
8^{-4} & \boxed{6}.4
\end{array}
$$

$$0.65_{10} = 0.5146_8 = 0.101001100110_2$$

Switches have two distinctive states "1" and "0". Each represents an output logic state. From the circuit of Fig. 1-1 (a) we can verify this principle.
In Fig. 1-1 (a),
When the switch is in position 1, LED2 will be ON.
When the switch is in position 2, LED1 will be ON.
When the switch is in position 0, both LED1 and LED2 will be ON.

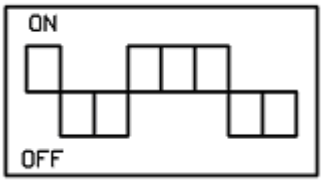
Switch logics could have two or three states: "1 "; "0"; and "X" or 'open'.
Relays can be used to demonstrate digital operations. The relay is triggered when the input voltage reaches the action voltage, when the input voltage drops below the release voltage, the relay will stop functioning.

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, Basic Logic Gates Experiment Module DLLT-EM01, and Digital Multimeter

EXERCISE

1. Make sure the Fault Simulator DIP Switch follows the below setting :



2. Insert connection clips according to Fig. 1-1 (a) to construct the circuit shown in Fig. 1-1 (b).

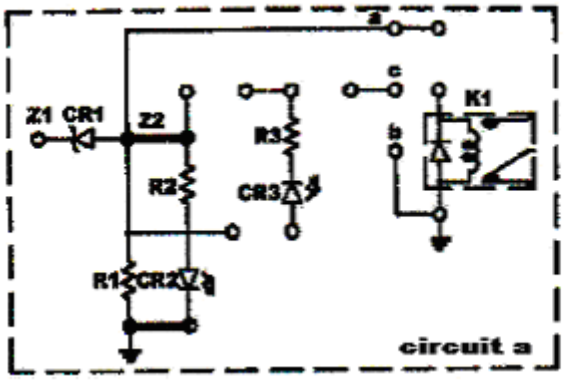


Fig. 1-1 (a)

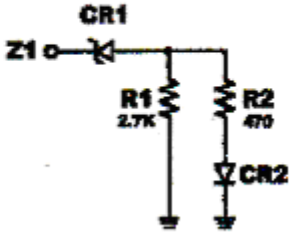
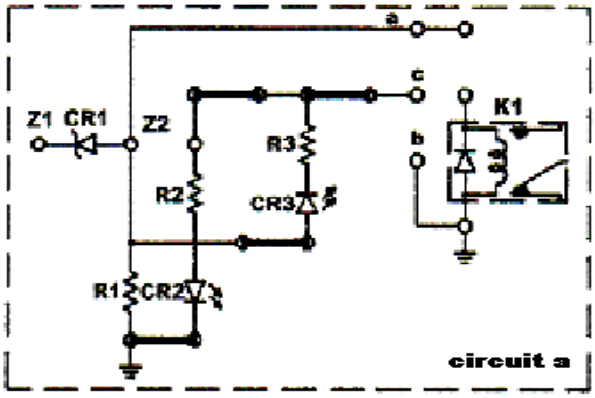


Fig. 1-1 (b)

3. Connect Z1 to the Adjustable Power Supply on DLLT-1300. Adjust the output voltage, measure the minimum and maximum voltage at Z2.

4. Adjust the output voltage and observe the LED (CR2).

5. Reconstruct the circuit according to Fig. 1-1 (c). Adjust the output voltage to 15V, Record the states of LED when the switch is in position a, b, c.



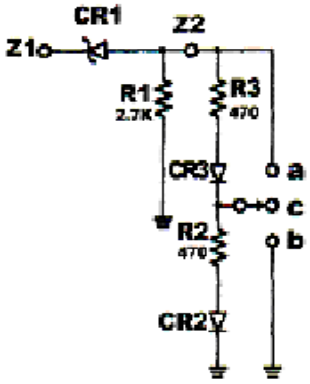


Fig. 1-1 (c)

6. Reconstruct the circuit according to Fig. 1-1 (d) and use the relay as a load. Increase the input voltage into the relay and observe the point at which the relay triggers. Decrease the input voltage and observe the release voltage.

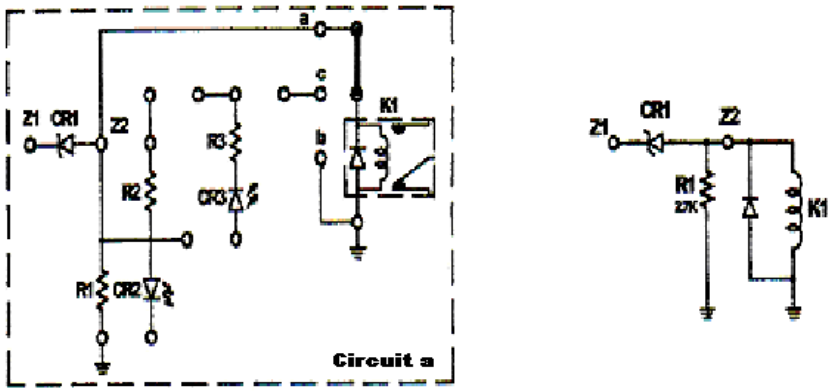


Fig.1-1(d)

RESULTS

1. The two points (or voltages) at which the LED is turned on and off can not be measured exactly.
2. The two points (or voltages) at which the relay triggers and releases can be measured exactly.
3. The action of the relay is a "digital" action.
4. When the switch is "closed", or connected to "+V", or connected to ground, it is in "floating" state and both CR1, CR2 are on.

1-2 Logic Gate Circuits

OBJECTIVES

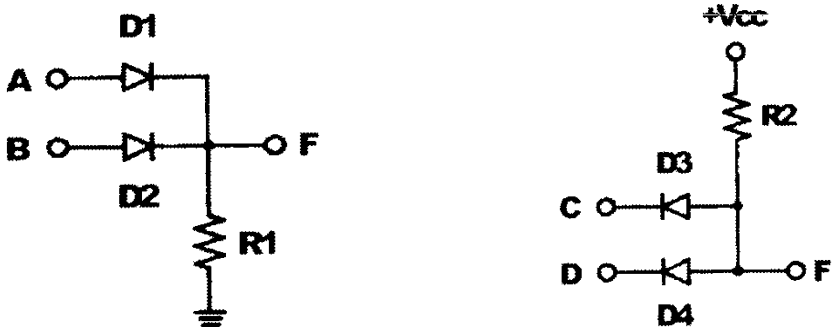
Understand the characteristics and principles of various logic gates.

DISCUSSIONS

Logic gates are constructed using two types of elements: the "Bipolar" and the "Metal Oxide Semiconductor" or MOS elements.

Bipolar logic elements include:

(1) Diode Logic, or "DL"

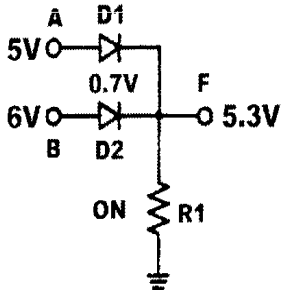


(a) OR gate (b) AND gate

Fig. 1-2-1 Diode Logic Gates

Refer to Fig. 1-2-1 (a), when the input voltage at either A or B is higher than the barrier voltage (0.7V) of the diode, there will be voltage at the output F. This is an "OR" logic gate. The value of A and B depends on the specifications of D1 and D2 as well as the output load.

If there are voltages at both A and B, the output voltage at F will be decided by the higher of two input voltages. For example, if A=5V and B=6V for the circuit of Fig. 1-2-2, the output F will be 5.3V so D1 is reversely non-conductive.



OFF

Fig. 1-2-2 OR gate

The inputs can be increased by simply adding diodes. Refer to Fig. 1-2-3.

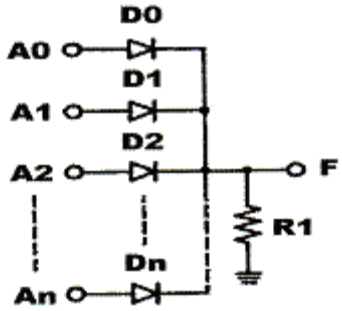


Fig. 1-2-3 "n"-input DL gate

In Fig. 1-2-1 (b), the lower of the two inputs C and D must be able to turn on D3 and D4, or + Vcc- Vc=0.7V or + Vcc- Vd=0.7V. Vc and Vd are the input voltages at C and D respectively.

If both C and D are low, the lower of the two will determine the output. In Fig. 1-2-4, Vcc= 10V, Vc= 6V and Vd= 8V.The output F is 6.7V, D3 will be on and D4 will be off. Circuits such as this is called an "AND" gate. To increase the input, refer to the connection shown in Fig. 1-2-4.

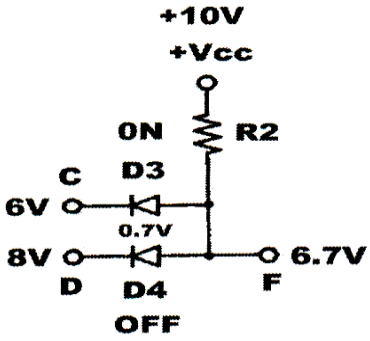
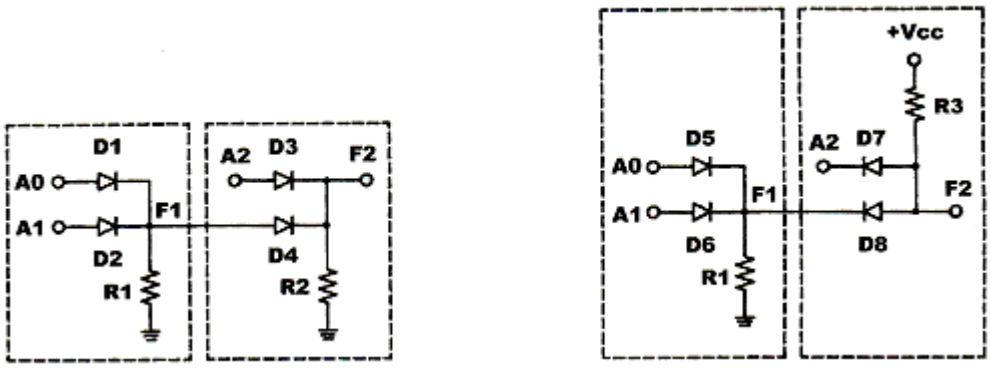


Fig .1-2-4 AND gate

EXAMPLE 1:
What happens when two DLs are connected in series, as in Fig. 1-2-5?



(a) OR-OR (b) OR-AND

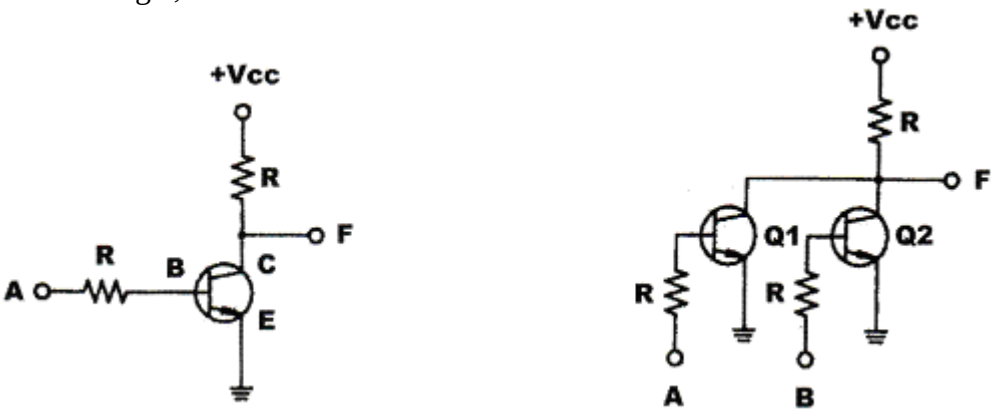
Fig. 1-2-5

ANSWER:

In Fig. 1-2-5 (a), F1 passes through D4 before reaching F2. The load resistors for F1 and F2 are R1 and R2 respectively. If D4 is on, R1 and R2 can be considered to be connected in parallel and the input current at A should increase, but the voltage at F2 will be 0.7V less than the voltage at F1.In Fig.1-2-5 (b), if both A0 and A1 are at low voltage, F1 should be 0V but with the addition of an AND gate there should be voltage drop at F1.

In order to make F1 close to 0V, R1 must be far smaller than R3 so that when F1 is at high voltage (almost reaching +V) D8 will be cut off. Obviously the circuit of Fig.1-2-5(b) is not an ideal connection as R1 has high power consummation.

(2) Resistor-Transistor Logic, or "RTL"



(a) NOT gate (b) NOR gate Fig. 1-2-6

Fig. 1-2-6

RTL logic utilizes the transistor's cutoff and saturation characteristics to generate high and low output voltages, or "1" and "0" logic state. Refer to Fig. 1-2-6 (a), when input A is high the output F will be low, when A is low F will be high so it is a "NOT" gate. In Fig. 1-2-6 (b), when one of the inputs A or B is high, the transistor will turn on and the output F will be low. F is high only when both A and B are tow so this is a "NOR" gate. When the circuits of Fig. 1-2-6 are used as driver circuit their output F are easily influenced by the magnitude of the load they are driving. Furthermore, one transistor is responsible for

both high and low state which will heat up the transistor considerably. The load carrying capacity of the output is quite low.

(3) Diode-Transistor Logic, or "DTL"

A typical DTL circuit is shown in Fig. 1-2-7.

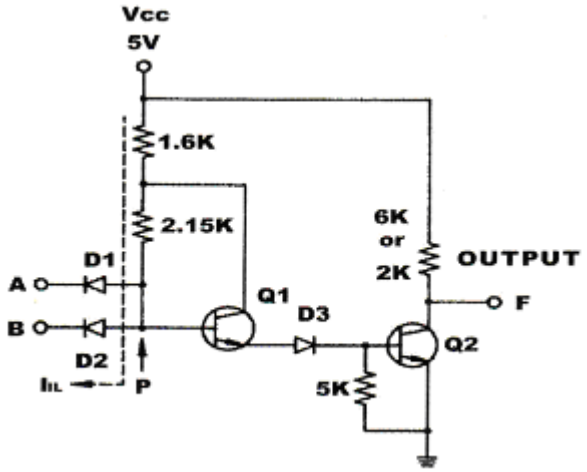


Fig. 1-2-7 DTL circuit

Refer to Fig. 1-2-7, when one of the inputs A or B is low, P will also be low, both Q1 and Q2 are off, and the output F will be low. Assuming the low input is 0.5V, voltage at P will be 1.2V (0.5V+0.7V). The current at D1 and D2, IIL= (5V-1.2V) x (1.65? + 2.155?) or 0.8mA. IIL is low current that the previous DTL must drive, limiting the previous DTL's output or "Fanout".

If both A and B are high then both Q1, Q2 will be on and the output F will be low (saturated Q2). Although DTL possesses transistor amplification, its structure is identical to RTL, so its voltage and current characteristics are also similar to the RTL.

(4) Transistor-Transistor Logic, or "TTL"

TTL replaces DTL with a unique characteristic: Under two different states 1 and 0, its output impudence is quite low. The circuit diagram of a TTL 7400 NAND gate is shown in Fig. 1-2-8.

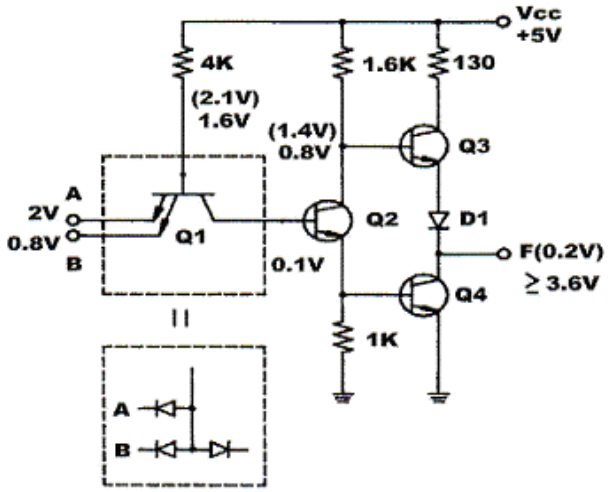


Fig. 1-2-8

The low and high input voltages for a standard TTL are limited to =-0.8V and =2V respectively. When one input is at 0.8V, a voltage of 0.1V exist at B pole of Q2, so Q4=off and Q3=on, and the output is high. If the input voltage is 2V, Q2's B pole has a voltage of 1.4V so Q2=on, Q3=off and the output is high.

Due to the effect of junction capacitance the speed of standard TTL is not vary fast. By adding a "Schottky Diode" between B and C pole of the transistor, speed of TTLs can be increased drastically. The Schottky diode has a forward bias of approximately 0.2V which increases the saturation voltage of transistor as well as its cutoff time. TTLs with added Schottky diode are called "High Speed TTL" and marked with letter "H" in their type number, such as 74HXX. Low power TTLs with Schottky diode are marked with LS, such as 74LSXX.

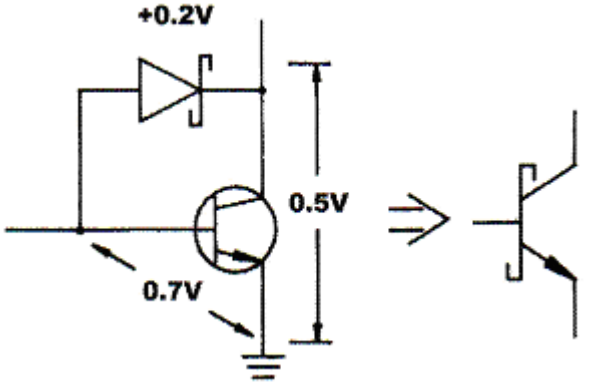


Fig. 1-2-9 Schottky transistor

A Schottky transistor is shown in Fig. 1-2-9.When it saturates the voltage at C and E is approximately 0.5V, the saturation is not too deep and operating speed is increased.

Unipolar MOS elements include:

(1) PMOS
(2) NMOS
(3) CMOS

An inverter made from NMOS is shown in Fig. 1-2-10.

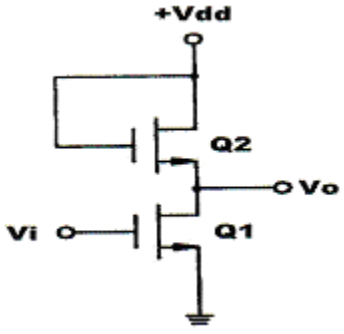


Fig. 1-2-10 NMOS inverter

In Fig. 1-2-10, Q2 is used as a load resistor and Q1 as an amplifier. Since the input impedance of MOSFET is very high (close to infinity), the output current is almost non-existent or only several + μ A. So MOS is highly capable of driving loads of the same type and has very high fanout.

CMOS, or "Complementary Metal Oxide Semiconductor", is made with P and N junctions. Atypical CMOS is shown in Fig. 1-2-11.

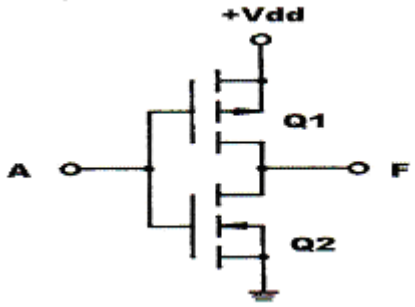


Fig. 1-2-11

In Fig. 1-2-11, when input A=1, Q2 is on and Q1 off so the output F=0. When A=0, the result is opposite as Q2 is off, Q1 is on and F=1. Clearly this is an inverter with Q1, Q2 responsible for 1 and 0 respectively. The output capability is increased significantly.

CMOS with buffer(s) are marked with letter "B" at the end of their type number. "LIB" means a CMOS without buffer. Fig. 1-2-12 shows symbol for CMOS with and without buffer(s).

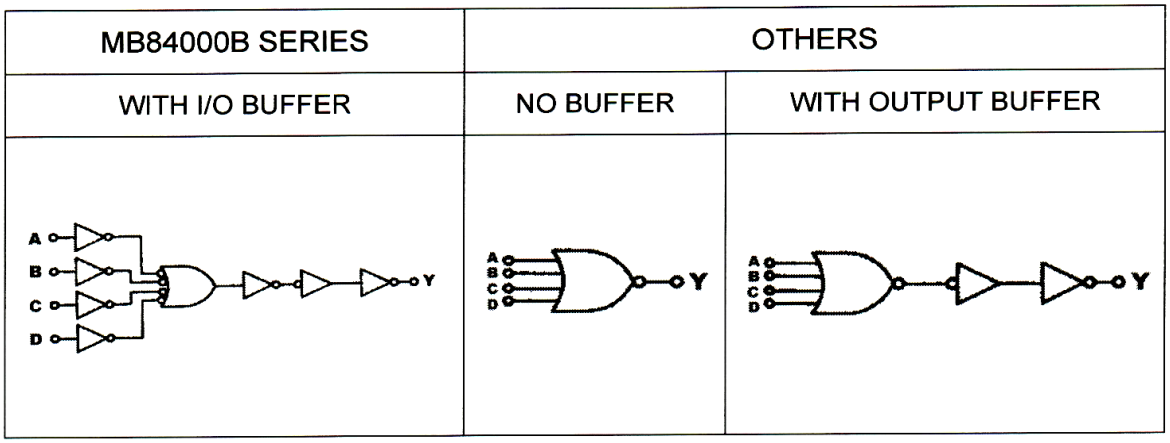


Fig. 1-2-12 IC gates with and without buffers

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, Basic Logic Gates Experiment Module DLLT-EM01, and Digital Multimeter

EXERCISE

(a) DL Circuit (DLLT-EM01 circuit c)

1. Insert connection clips according to Fig. 1-2 (a) to construct the equivalent DL circuit above.

2. Connect inputs D1, D2 to the 1.5V- 15V output of the Adjustable Power Supply. Use the circuit of Fig. 1-1 (a) to reduce and limit the input voltage to between 0V and 5V.

3. Connect D1, D2 to Data Switches SW0 and SW1 respectively. Follow the 2 input sequences below, measure and record the output voltages at F10.

①

D2	D1	F10
⏚	0V	
⏚	0.2V	
⏚	0.4V	
⏚	0.6V	
⏚	0.8V	
⏚	1V	
⏚	2V	
⏚	3V	
⏚	4V	
⏚	5V	

②

D2	D1	F10
0V	⏚	
0.2V	⏚	
0.4V	⏚	
0.6V	⏚	
0.8V	⏚	
1V	⏚	
2V	⏚	
3V	⏚	
4V	⏚	
5V	⏚	

Are the outputs different when one of the inputs is open?

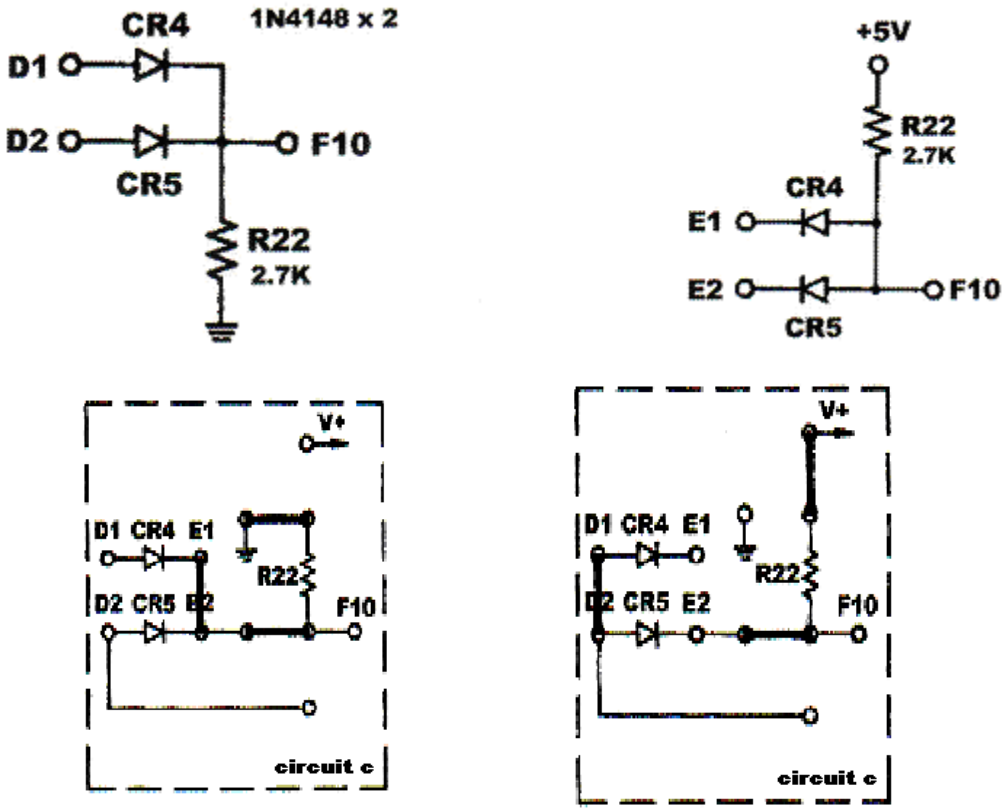


Fig. 1-2(a) Fig. 1-2(b)

4. Rearrange the connection clips according to Fig. 1-2 (b).

5. Connect +V to the +5V output of Fixed Power Supply. As in step 2, limit the input voltages to 0V-5V for inputs E1, E2.

6. Connect E1, E2 to Data Switches SW2 and SW3 respectively. Follow the 2 input sequences below, measure and record the output voltages at F10.

①

E2	E1	F10
+V	0V	
+V	2V	
+V	3V	
+V	4V	
+V	5V	

②

E2	E1	F10
0V	+V	
2V	+V	
3V	+V	
4V	+V	
5V	+V	

(b) RTL Circuit (DLLT-EM01 circuit b)

1. Insert connection clip between R5 and +V. Connect +V to the +5V output of the Fixed Power Supply.

2. Limit the input voltages for H1 to between 0V and 5V. Starting from 0V measures and records the output at F11.Increase the input voltage in increment of 0.1V and records each corresponding output.

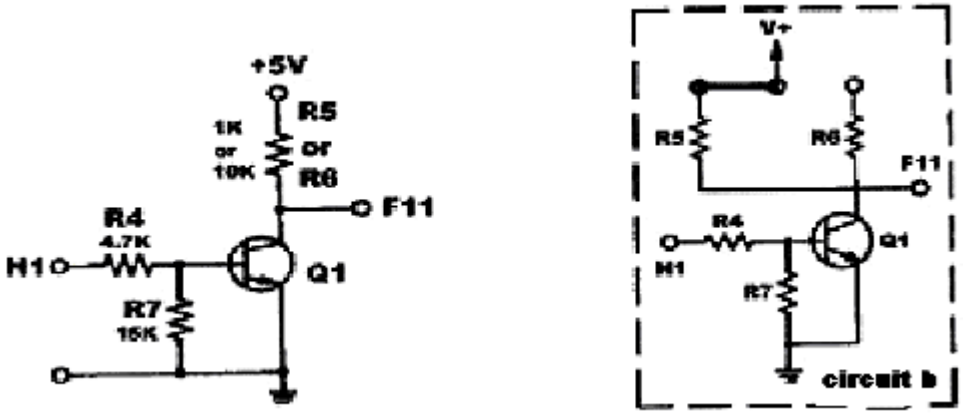


Fig 1.2c

H1	F11	H1	F11	H1	F11	H1	F11	H1	F11
0V		1.1V		2.1V		3.1V		4.1V	
0.2V		1.2V		2.2V		3.2V		4.2V	
0.3V		1.3V		2.3V		3.3V		4.3V	
0.4V		1.4V		2.4V		3.4V		4.4V	
0.5V		1.5V		2.5V		3.5V		4.5V	
0.6V		1.6V		2.6V		3.6V		4.6V	
0.7V		1.7V		2.7V		3.7V		4.7V	
0.8V		1.8V		2.8V		3.8V		4.8V	
0.9V		1.9V		2.9V		3.9V		4.9V	
1V		2V		3V		4V		5V	

3. Replace R5 (1KΩ) with R6 (10KΩ) by moving the connection clip to the right side. Repeat the measurement step2.

H1	F11	H1	F11	H1	F11	H1	F11	H1	F11
0V		1.1V		2.1V		3.1V		4.1V	
0.2V		1.2V		2.2V		3.2V		4.2V	
0.3V		1.3V		2.3V		3.3V		4.3V	
0.4V		1.4V		2.4V		3.4V		4.4V	
0.5V		1.5V		2.5V		3.5V		4.5V	
0.6V		1.6V		2.6V		3.6V		4.6V	
0.7V		1.7V		2.7V		3.7V		4.7V	
0.8V		1.8V		2.8V		3.8V		4.8V	
0.9V		1.9V		2.9V		3.9V		4.9V	
1V		2V		3V		4V		5V	

(c) DTL Circuit (DLLT-EM01 circuit c/b)

1. Connect the DL circuit of circuit c with the RTL circuit of circuit b according to Fig. 1-2 (d) with a test lead. Insert connection clips as marked. Connect +V of circuit b to the +5V output of Fixed Power Supply.

2. Limit the input voltages for D1, D2 to 0V~5V. Follow the input sequences below, measure and record outputs at F10 and F11.

D2	D1	F10	F11	D2	D1	F10	F11	D2	D1	F10	F11
⏚	0V			⏚	2.4V			⏚	4.4V		
⏚	0.6V			⏚	2.6V			⏚	4.6V		
⏚	0.8V			⏚	2.8V			⏚	4.8V		
⏚	1V			⏚	3V			⏚	5V		
⏚	1.2V			⏚	3.2V						
⏚	1.4V			⏚	3.4V						
⏚	1.6V			⏚	3.6V						
⏚	1.8V			⏚	3.8V						
⏚	2V			⏚	4V						
⏚	2.2V			⏚	4.2V						

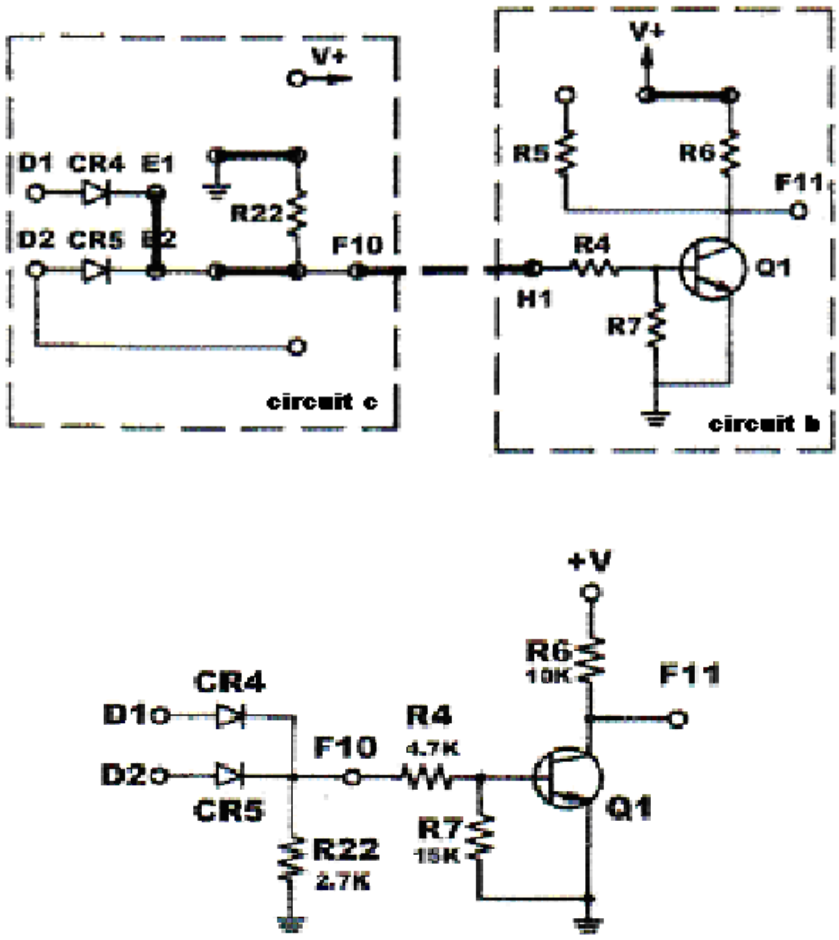


Fig. 1-2(d)

(d) TTL Circuit (DLLT-EM01 circuit d)

1. Insert connection clips according to Fig. 1-2 (e). U1 is a standard series 7400 NAND gates while U2 is a LS series 74L02 NOR gate.

2. Connect +5V output of Fixed Power Supply to +5V on circuit d.

3. Limit the input voltages for A1 to 0V~5V. Follow the input sequences below, measure and record outputs at F1.

4. Limit the input voltages for A3 to 0V~5V. Follow the input sequences below, measure and record outputs at F2.

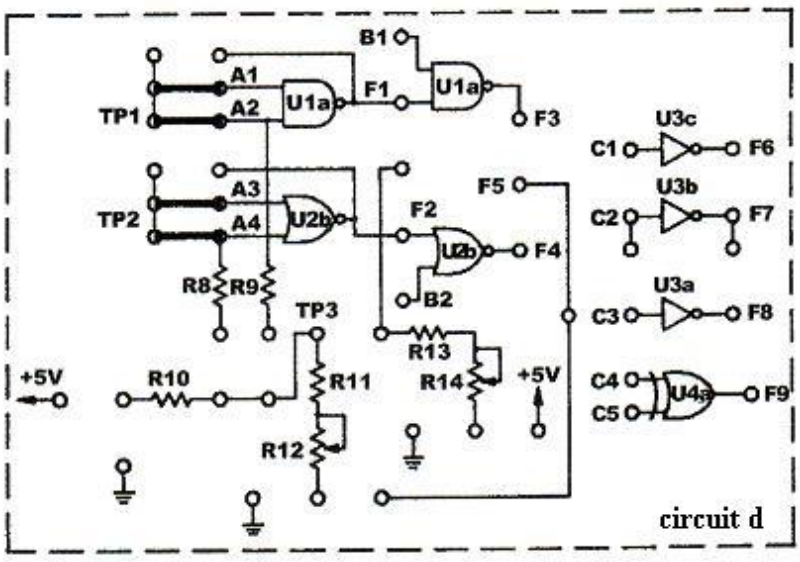


Fig. 1-2 (e)

A1	F1	A1	F1	A1	F1	A1	F1	A1	F1
0V		1.5V		2.5V		3.5V		4.5V	
0.6V		1.6V		2.6V		3.6V		4.6V	
0.7V		1.7V		2.7V		3.7V		4.7V	
0.8V		1.8V		2.8V		3.8V		4.8V	
0.9V		1.9V		2.9V		3.9V		4.9V	
1V		2V		3V		4V		5V	
1.1V		2.1V		3.1V		4.1V			
1.2V		2.2V		3.2V		4.2V			
1.3V		2.3V		3.3V		4.3V			
1.4V		2.4V		3.4V		4.4V			

A3	F2	A3	F2	A3	F2	A3	F2
1V		2V		3V		4V	
1.1V		2.1V		3.1V		4.1V	
1.2V		2.2V		3.2V		4.2V	
1.3V		2.3V		3.3V		4.3V	
1.4V		2.4V		3.4V		4.4V	
1.5V		2.5V		3.5V		4.5V	
1.6V		2.6V		3.6V		4.6V	
1.7V		2.7V		3.7V		4.7V	
1.8V		2.8V		3.8V		4.8V	
1.9V		2.9V		3.9V		4.9V	
2V		3V		4V		5V	

(e) CMOS Circuit (DLLT-EM01 circuit e)

1. Insert connection clips according to Fig. 1-2 (f). U5 is a standard series CMOS CD4011. Connect VDD to +12V output of the Fixed Power Supply.

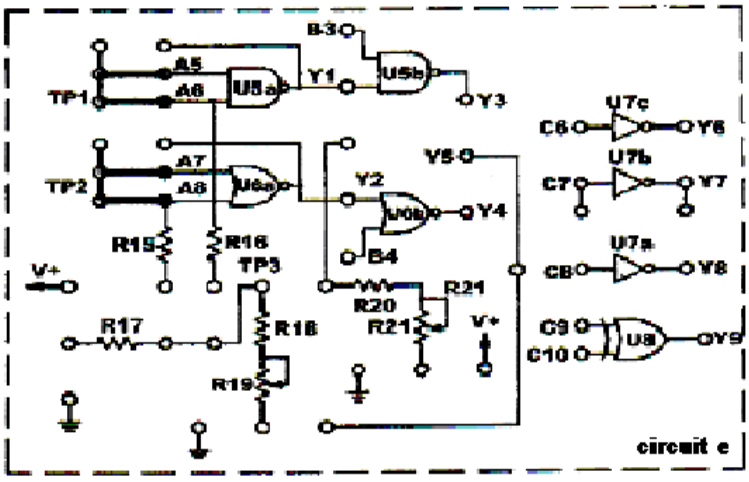


Fig. 1-2 (f)

2. Increase the input voltages for A5 in increments of 0.5V, starting from 0V.Measure and record each corresponding output voltage at Y1 below:

A5	Y1	A5	Y1	A5	Y1	A5	Y1
0V		3.5V		7V		10.5V	
0.5V		4V		7.5V		11V	
1V		4.5V		8V		11.5V	
1.5V		5V		8.5V		12V	
2V		5.5V		9V			
2.5V		6V		9.5V			
3V		6.5V		10V			

3. U6 is a 74HC02 high-speed CMOS gate.

4. Increase the input voltages for A7 in increments of 0.5V, starting from 0V. Measure and record each corresponding output voltage at Y2 below.

A7	Y2	A7	Y2	A7	Y2	A7	Y2
0V		3.5V		7V		10.5V	
0.5V		4V		7.5V		11V	
1V		4.5V		8V		11.5V	
1.5V		5V		8.5V		12V	
2V		5.5V		9V			
2.5V		6V		9.5V			
3V		6.5V		10V			

RESULTS

1. The following logic gates have very precise "HIGH" or "LOW' states:
   (a) TTL
   (b) LS series TTL (c) CMOS
   (d) HC series CMOS

2. The following logic gates do not have very precise "HIGH" or "LOW' states:
   (a) DL
   (b) RTL
   (c) DTL

3. TTL measurements taken in this experiment should be close to these theoretical values:

$$V_{IL} \leq 0.8\text{V}; \quad V_{IH} \geq 2\text{V}; \quad V_{OL} \leq 0.4\text{V}; \quad V_{OH} \geq 2.4\text{V};$$

4. CMOS measurements taken in this experiment should be close to these theoretical values:

$$V_{IL} \leq 30\%\ \text{VDD}; \quad V_{IH} \geq 70\%\text{VDD}; \quad V_{OL} \leq 10\%\text{VDD}; \quad V_{OH} \geq 90\%\text{VDD}$$

FAULT SIMULATION

The output F11 of the RTL circuit remains high regardless of the input state at H1. What could be the problem(s)?

1-3 Threshold Voltage Measurement

OBJECTIVE

Understand the relationship between equivalent input/output voltages.

DISCUSSION

Threshold Voltage:

Threshold voltage, or VT, is the voltage at which the input and output voltage are equal. The circuit will change state if the input voltage is higher or the output voltage is lower than VT. The value of VT varies, depending on the type of logic gate. In this experiment we will perform measurements on TTL standard and LS series gates, as well as CMOS standard and HC series gates.

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, DLLT-EM01: Basic Logic Gates Experiment Module, and Digital Multimeter

EXERCISE

(a) TTL Threshold Voltage Measurement (DLLT-EM01 circuit d)

1. Using U1a in the circuit of Fig. 1-3 (a), connect the input to the output. Measure the Voltage at A1 and F1 with the multimeter.

2. Using U2a in the circuit of Fig. 1-3 (a), connect the input to the output. Measure the Voltage at A3 and F2 with the multimeter.

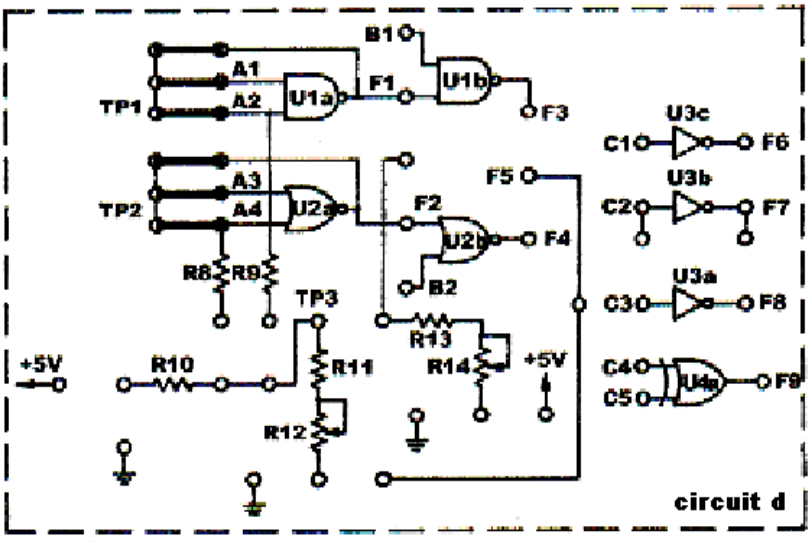


Fig. 1-3 (a)

(b) CMOS Threshold Voltage Measurement (DLLT-EM01 circuit e)

1. Using U5a in the circuit of Fig. 1-3 (b), connect the input with the output. Measure the voltage at A5 and Y1 with the multimeter.

2. Using U6a in the circuit of Fig. 1-3 (b), connect the input with the output. Measure the voltage at A7 and Y2 with the multimeter.

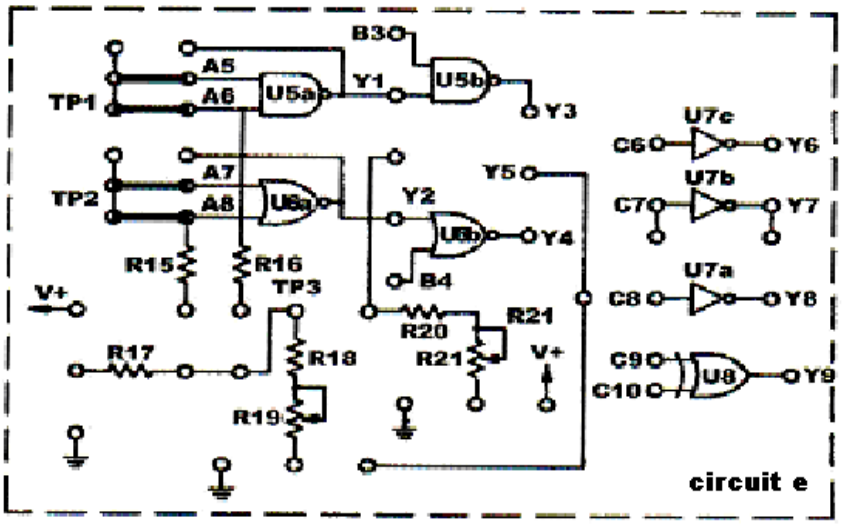


Fig. 1-3 (b)

RESULTS

1. Compare VT for standard and LS series TTL gates. Are there any differences?

2. Compare VT for standard and HC series CMOS gates. Are there any differences?

1-4 Voltage/Current Measurement

OBJECTIVE

Understand the voltage and current characteristics of TTL CMOS gates.

DISCUSSION

From the rated voltages: $V_{IL} \leq 0.8V$; $V_{IH} \geq 2V$; $V_{OL} \leq 0.4V$; $V_{OH} \geq 2.4V$; we can determine its rated current values I_{IH}; I_{IL}; I_{OH}; I_{OL}.

The rated voltages will affect the accuracy of output logic level while the current values will affect the gate's ability to drive external loads.

In this experiment we will measure and compare voltage as well current values of various logic gates. To achieve higher accuracy, try to record as many decimal points as possible when measuring voltages and currents.

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, DLLT-EM01: Basic Logic Gates Experiment Module, Digital Multimeter

EXERCISE

(a) TTL I/O Voltage and Current Measurement (DLLT-EM01 circuit d)

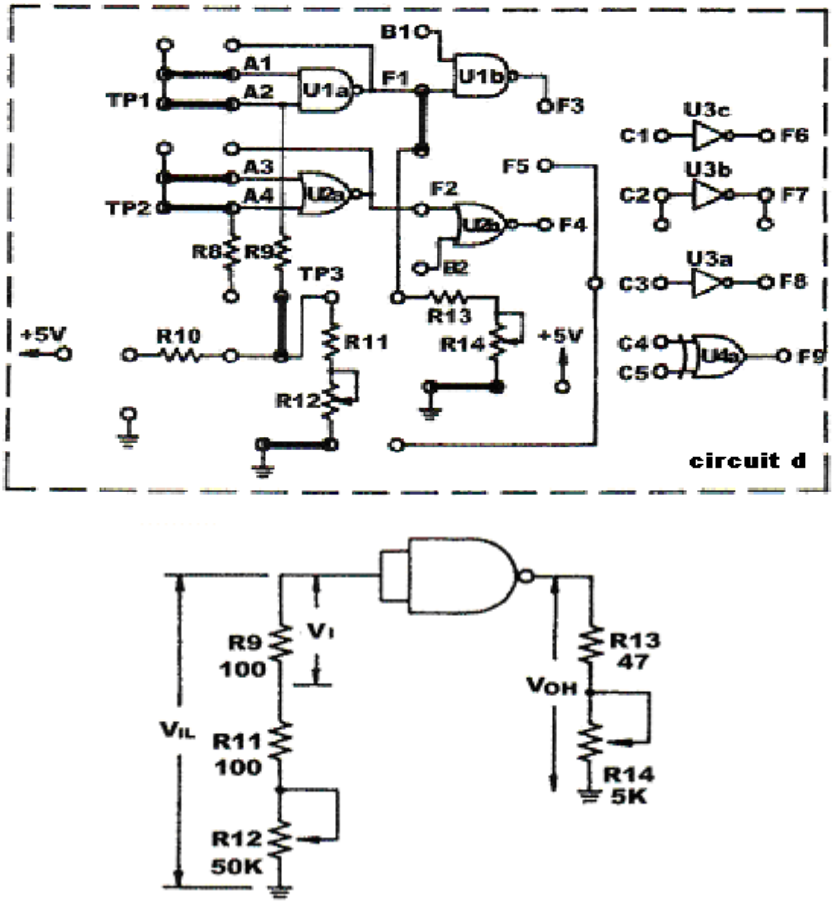


Fig. 1-4 (a)

1. Insert connection clips according to Fig. 1-4 (a). Connect TP1 to a data switch and switch it to 0.

2. Using U1a for this section, adjust R12 So V_{IL}=0.8V.Measure voltage across A2 and TP3. Vi= _____ V.I_{IL}=Vi/100= _____ mA. Adjust R14 to find V_{OH} and V_{OL}.

3. Adjust R14 to set V_{OH} to 2.4V and remove the connection clip between R14 and ground. Measure the value of I_{OH}. I_{OH}= _____ mA.

4. Remove the connection clips between R9-TP3 and F1-R13; place them between R8-TP3 and F2-R13.

5. Connect TP2 to a data switch and switch it to 0. Measure U2a's voltage and current characteristics. Set V_{IL} to 0.8V and measure the voltage (V2) between A3 and TP3. Calculate I_{IL}=V2/100= _____ mA. Adjust R14 to find V_{OH} and V_{OL}.

6. Adjust R14 to set V_{OH} to 2.4V and remove the connection clip between R14 and ground. Measure the current (I_{OH}) between R14 and ground. I_{OH} = _____ mA.

7. Insert connection clips according to Fig. 1-4 (b). Adjust R12 to set the voltage (V_{IH}) between TP3 and ground to 2V. Measure the voltage (V2) between A2 and TP3. V2/100=1_{1H}= _____ mA.

8. Adjust R12 and measure V_{OL}, V_{oH}. Adjust R14 SO V_{OL} =0.4V, remove the connection clip between R14 and Vcc. Measure the current ($IoL_)$ between Vcc and R14. I_{OL}= _____ mA.

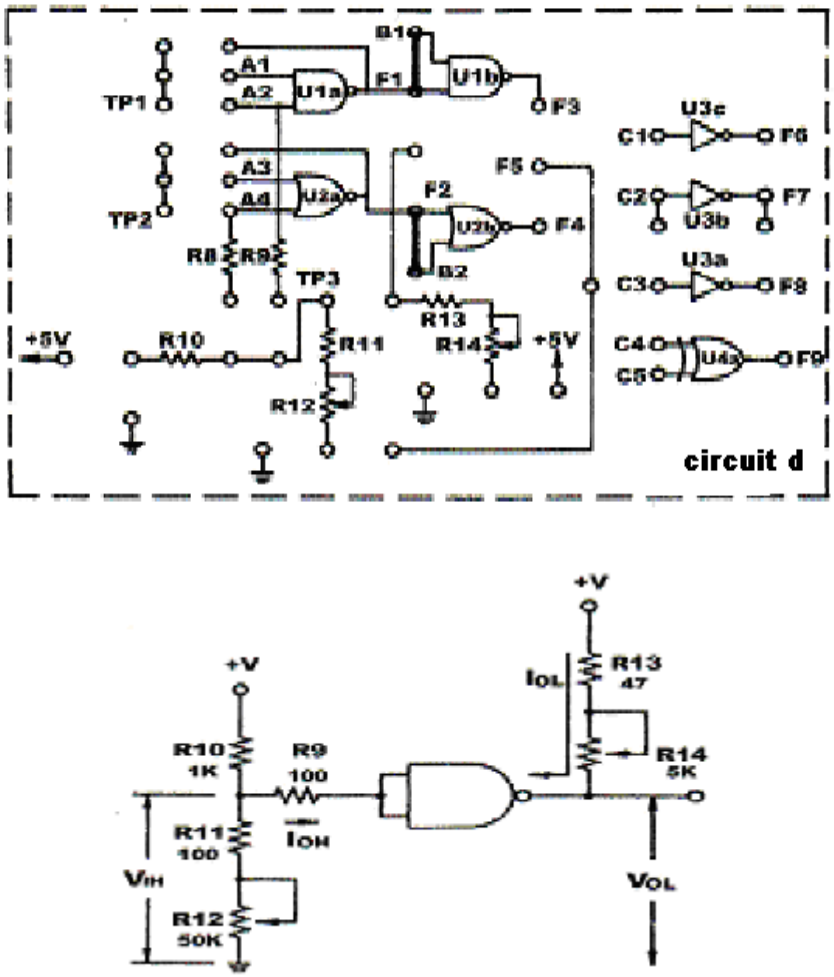


Fig. 1-4 (b)

1. Remove the connection between R9-R10 and F1-R13 and place them between R8-R10 and F2-R13 respectively. Adjust R12 so the voltage (V_{IH}) is 2V. Measure the voltage V2 between A3 and TP3.

V2/100=1_{1H}=_____ mA.

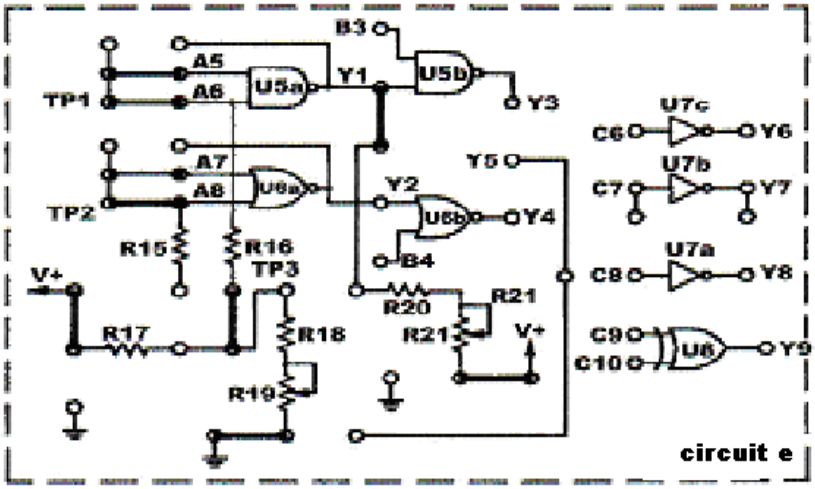
2. Adjust R14 and measure V_{OL}, V_{OH}. Adjust R14 So V_{OL} =0.4V. Remove the connection clip between R14 and ground, measure the current I_{OL}. I_{OL}=_____ mA.

(b) CMOS Voltage and Current Measurement (Module DLLT-EM01 circuit d)

1. Insert connection clips according to Fig. 1-4 (c). U5a will be used in this section. Connect V+ to +12V. Connect TP1 to a data switch and switch it to 0.

2. Adjust R19 so the voltage V_{IL} between TP3 and ground is 3.6V. Adjust R21 and measure the maximum and minimum voltage at Y1. Measure the voltage V3 between R19 and TP3. V3/100=1_{1L}= _____ mA. Adjust R21 to set the voltage V_{OH} between Y1 and ground to 10.8V. Remove the connection clip between R21 and ground, measure the current IoL between R21 and ground. I_{OL}= _____ mA.

3. Adjust R19 so the voltage V_{IH} between TP3 and ground is 8.4V. Remove the connection clip between R21-ground, place it between R21-V+. Adjust R21 and measure the maximum and minimum voltage at Y1. Measure the voltage V4 between A5 and TP3. V4/100=1_{1H}= ___ mA. Adjust R21 so the voltage V_{OL} between Y1 and ground is 1.2V. Measure the current I_{OL} between R21 and Vcc. I_{OL}= _____ mA.



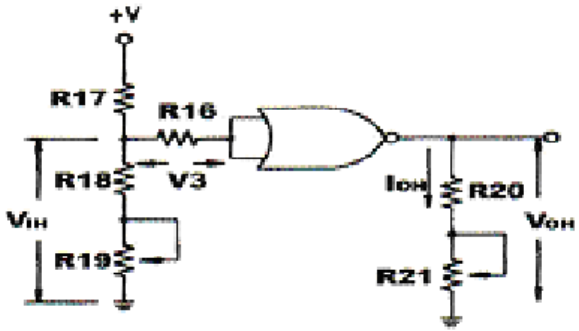


Fig. 1-4 (c)

RESULTS

1. CMOS input voltages $V_{IL} \leq$ 30% Vdd; $V_{IH} \geq$30%Vdd; output voltages $V_{OL} \leq$10%Vdd; $V_{OH} \geq$90%Vdd; When the output load is open V_{OH}=Vdd, V_{OL}=OV.

2. Due to its higher resistance value the LS series TTL gates have lower input current than the standard series TTL gates. Their output currents are about equal.

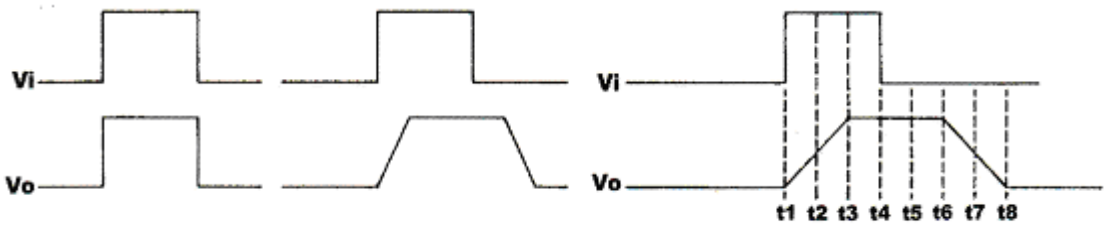
1-5 Basic Logic Gate Transmission Delay Measurements

OBJECTIVE

Understand the phenomenon of logic gate transmission delay.

DISCUSSION

An integrated circuit, or "IC", contains components such as resistors; semiconductors; capacitors and other devices. When a signal changes state inside an IC, the IC will go through cycles of charge-discharge. The time required to rising from 10% of the maximum voltage to 90% of the maximum voltage is referred to as the "Rise Time" while the time required to fall from 90% of the maximum voltage down to 10% of the maximum voltage is called "Fall Time". Square waves are used to compare the delay time between input and output. 50% of the maximum value is used as the reference point.



(a) NO DELAY (b) SMALL DELAY (c) LONG DELAY

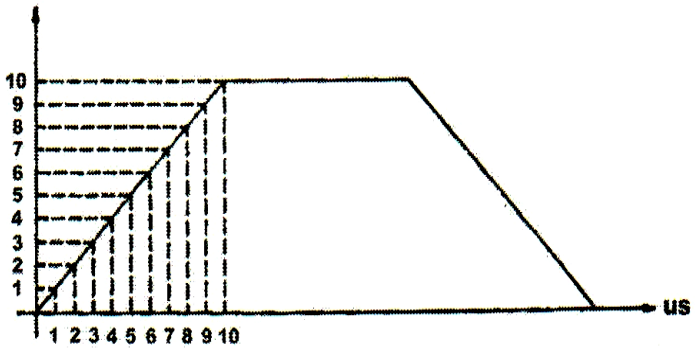
Fig. 1-5

In cases where cycle of the input frequency is higher than the delay time of a logic gate, characteristics of the logic gate will be changed. For example, an inverter gate that is suppose to reverse the phase of input will not have enough time to perform this task because the cycle is too fast. Instead of completely reversing the phase of input, in some sections the output will remain in the same phase as the input, rendering gate useless.

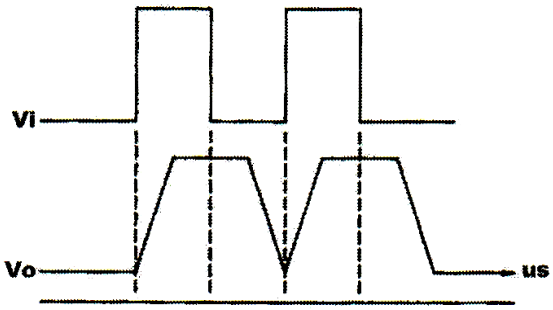
Fig. 1-5 (a) shows the ideal transmission of data without any delay.
In Fig. 1-5 (b), a small amount of delay is present.
Fig. 1-5 (c) shows a long delay between the input and output. The input reached its maximum value at t1 while the output remains low due to the gate delay.

At t4, where the input drops, the output is still high. During t3~t4 the input and output are equal. From t4 to t6 the input and output are in opposite phase. At t8, the output finally catches up with the input. Such long delay is very unpractical in actual applications but demonstrates the principles of delay very clearly.

As mentioned in the first paragraph, rise time or "Tr", is the amount of time required to go from 10% to 90% of the maximum voltage? Therefore, we can calculate Tr for the graph shown below as
Tr = 90% t -10%t = 9µs - 1 µs = 8µs.



The delay time for the graph below is 50% of the time required to reach the maximum value or 3μs.



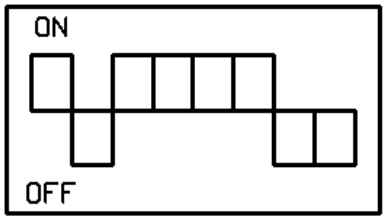
EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM01: Basic Logic Gates Experiment Module; Oscilloscope; and Digital Multimeter.

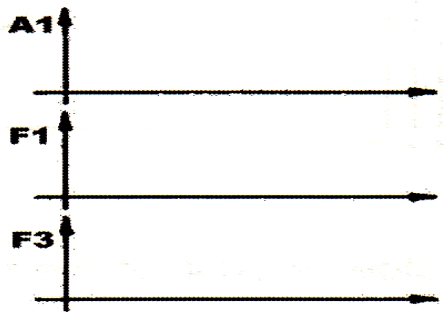
EXERCISE

(a) TTL Gate Delay Time Measurement

1. Make sure the Fault Simulator DIP Switch follows the below setting :

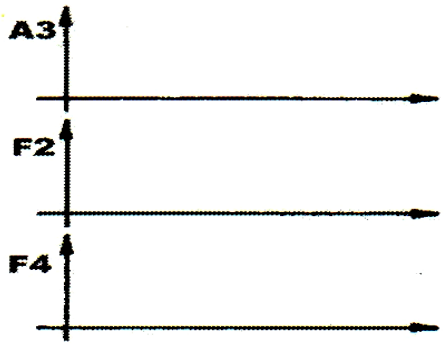


2. Insert connection clips according to Fig. 1-5 (a). U1a and U1b will be used in this step. Connect input A1 to the TTL level output of Clock Generator and select 100KHz. Measure and record waveforms of A1, F1, and F3 with an oscilloscope.



What is the delay time for F1 and F3?

3. U2a and U2b are used in this step and A3 is the input. Connect A3 to 100 KHz TTL output of Clock Generator, measure and record waveforms at A3, F2, and F4.



What is the delay time for F2 and F4?

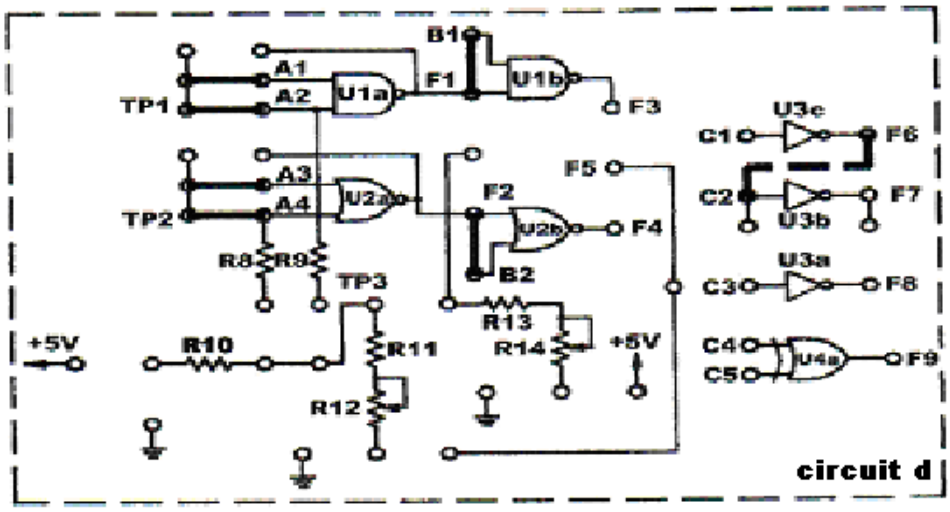
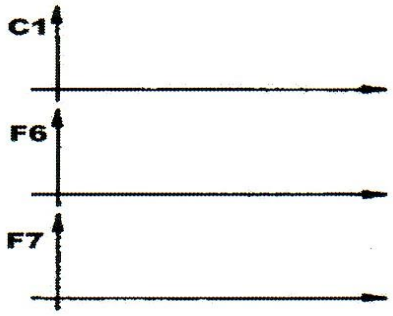


Fig. 1-5 (a)

4. U3c is used in this step and C1 is the input. Connect C1 to 1 MHz TTL output of Clock Generator, measure and record waveforms at C1, F6, and F7.

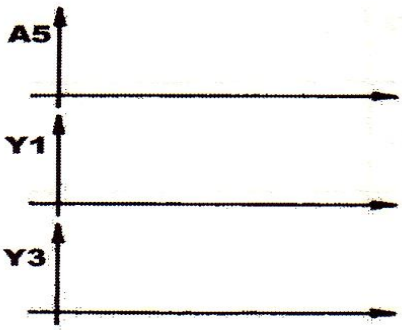


What is the delay time for F6 and F7?

(b) CMOS Gate Delay Time Measurements

1. Insert connection clips according to Fig. 1-5 (b), connect Vdd to +12V.

2. U5a and U5b are used in this step and A5 is the input. Connect A5 to 10KHz CMOS level output of Clock Generator, measure and record waveforms at A5, Y1, and Y3. A5 Y1 Y3



What is the delay time for Y1 and Y3?

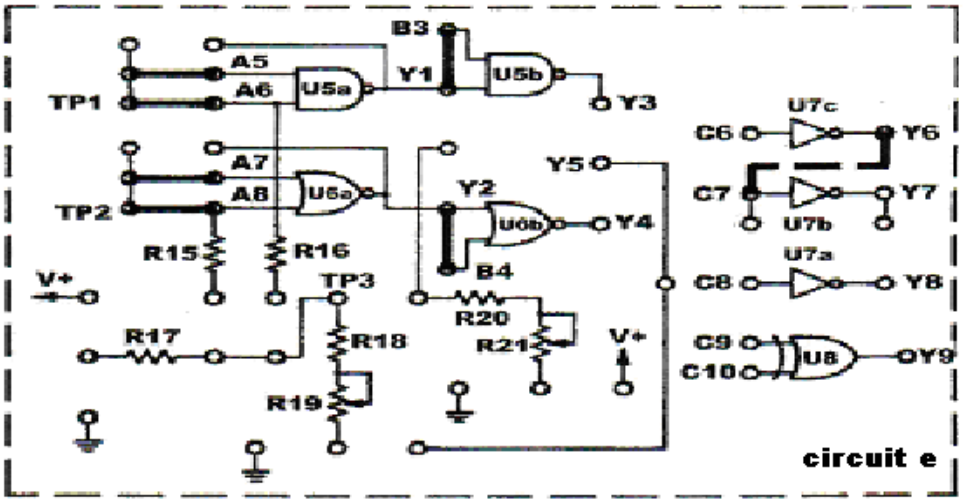
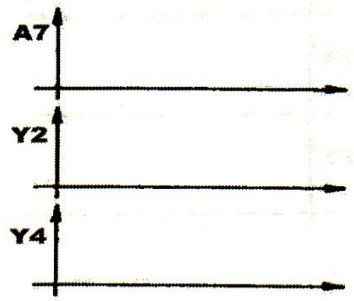


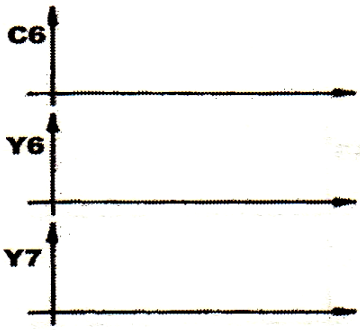
Fig. 1-5 (b)

3. U6a and U6b are used in this step and A7 is the input. Connect A7 to 100KHz CMOS output of Clock Generator, measure and record waveforms at A7, Y2, and Y4.



What is the delay time for Y2 and Y4?

4. U7b and U7c are used in this step and C6 is the input. Connect C6 to 100KHz CMOS output of Clock Generator, measure and record waveforms at C6, Y6, and Y7.



What is the delay time of Y6 and Y7?

RESULTS

1. How does the rise and fall time of Standard; LS series and Schmidt type TTL gates compare with each other? What about their delay times?

2. Which series of CMOS gate has higher rise and fall time? Standard series or HS series?

1-6 Measurements of Basic Logic Gates Characteristics

OBJECTIVE

Understand the symbols and characteristics of various basic logic gates.

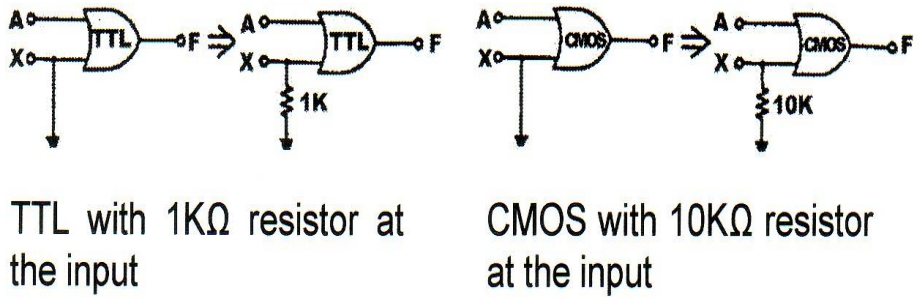
DISCUSSIONS

The input and output characteristics of basic logic gates are defined below:

V_{OH}	- High output voltage	I_{OH}	- High output current
V_{OL}	- Low output voltage	I_{OL}	- Low output current
V_{IH}	- High input voltage	I_{IH}	- High input current
V_{IL}	- Low input voltage	I_{IL}	- Low input current

Characteristics of TTL gates are different from those of CMOS gates. The load and current-limiting resistors they are connected to are different as well. For example, in the case of an OR gate and an AND gate:

1. **OR gate**: inputs of TTL are connected to a 1 KΩ resistor while inputs of CMOS gates are connected to a 10KΩ resistor.



TTL with 1KΩ resistor at the input

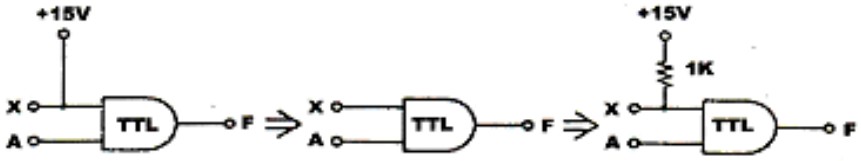
CMOS with 10KΩ resistor at the input

TTL with 1 KΩ resistor at the input CMOS with 10KΩ resistor at the input

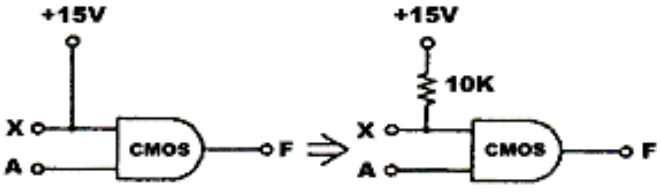
Resistance for the LS series TTL is approximately 5KΩ. If the X input of a TTL OR gate is grounded then the output F is equal to the input A (F=A), making expansion control impossible.

If the resistor is grounded and there is no signal at X, then X is equivalent to being grounded and F=A. If necessary a signal could be added to X so that F=AxX. The output can be controlled by X.

2. **AND gate**: TTL AND gates are in high state when it is open or when a resistor is connected to the supply voltage. CMOS AND gates are in high state when a resistor of at least 1 0K S2 is connected to the supply voltage.



"HIGH" TTL and gate



"HIGH" CMOS AND gate

The "Truth Table" is a table that shows a logic gate's corresponding inputs and outputs under ideal conditions.

1. OR gate

STATE	INPUT		OUTPUT	
	A	B	F	
0	0	0	0	When A=0, B=0 the output F=0
1	0	1	1	When A=0, B=1 the output F=1
2	1	0	1	When A=1, B=0 the output F=1
3	1	1	1	When A=1, B=1 the output F=1

In Boolean expression, F= $\bar{A}\,B + A\,\bar{B}$ + A B= A+B

2. AND gate

STATE	INPUT		OUTPUT	
	A	B	F	
0	0	0	0	When A=0, B=0 the output F=0
1	0	1	0	When A=0, B=1 the output F=0
2	1	0	0	When A=1, B=0 the output F=0
3	1	1	1	When A=1, B=1 the output F=1

In Boolean expression, F=AB

3. INVERTER gate

STATE	INPUT	OUTPUT	
	A	F	
0	0	1	When A=0, the output F=1
1	1	0	When A=1, the output F=0

In Boolean expression, F= $\bar{A}$

4. XOR gate

STATE	INPUT		OUTPUT
	A	B	F
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

When A=B, the output F=0
When A ≠ B, the output F=1

In Boolean expression, F= $\bar{A}$B + A$\bar{B}$ = A ⊕B

5. NAND gate

The output of a NAND gate is the exact opposite of an AND gate.

STATE	INPUT A	INPUT B	OUTPUT F	
0	0	0	0	When A=0, B=0 the output F=1
1	0	1		When A=0, B=1 the output F=1
2	1	0		When A=1, B=0 the output F=1
3	1	1		When A=1, B=1 the output F=0

In Boolean expression, F= $\overline{AB}$

6. NOR gate

The output of a NOR gate is the exact opposite of an OR gate.

STATE	INPUT A	INPUT B	OUTPUT F	
0	0	0	1	When A=0, B=0 the output F=1
1	0	1	0	When A=0, B=1 the output F=0
2	1	0	0	When A=1, B=0 the output F=0
3	1	1	0	When A=1, B=1 the output F=0

In Boolean expression, F= $\overline{\overline{A+B}} = \bar{A} \times \bar{B}$

These truth tables are based on "positive" logic where positive voltage represents "1" and negative voltage represents "0". In case negative logic is used the output will be reversed.

Compare the truth tables for a positive and a negative OR gate shown below:

STATE	INPUT A	INPUT B	OUTPUT F
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	1

STATE	INPUT A	INPUT B	OUTPUT F
0	1	1	1
1	1	0	0
2	0	1	0
3	0	0	0

Observe the truth table for a negative logic OR gate. It to equivalent to a positive logic AND gate.

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM01: Basic Logic Gates Experiment Module; and Oscilloscope

EXERCISE

(a) AND Gate Characteristics Measurement (DLLT-EM01 circuit d)

1. Insert connection clips according to Fig. 1-6. U1a and U1b will be used in this section.

2. Connect inputs A1, A2 to Data Switch SW0, SW1 TTL level and output F3 to Logic Indicator L0. Follow the input sequences below and record the outputs.

STATE	INPUT		OUTPUT
	A2	A1	F3
0	0	0	
1	0	1	
2	1	0	
3	1	1	

3. Connect A4 to the 10Hz TTL level output of Clock Generator. Measure and record the input and output waveforms.

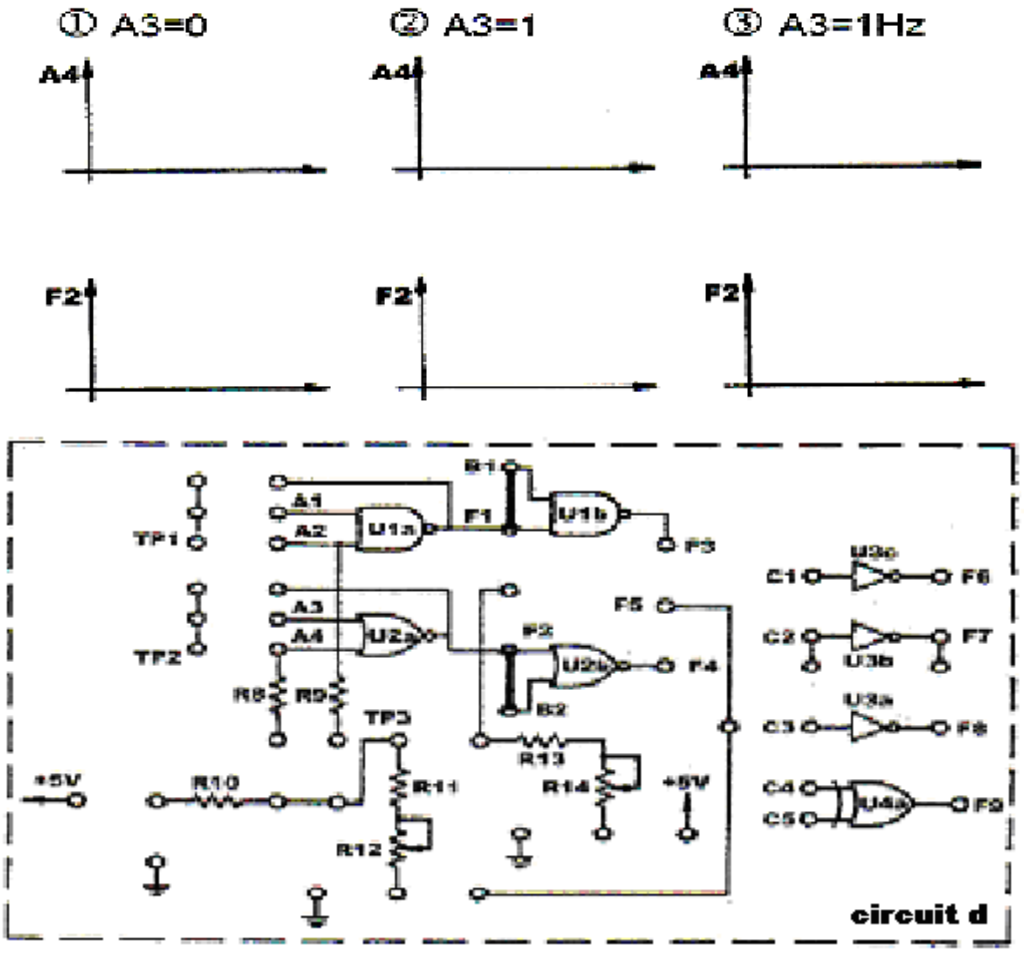


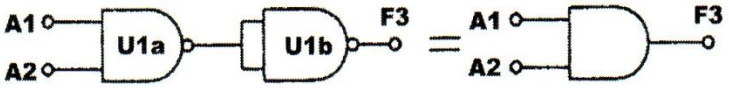
Fig. 1-6 STATE

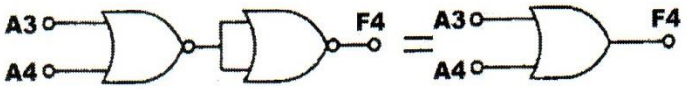
(b) OR Gate Characteristics Measurement (DLLT-EM01 circuit d)

1. U2a and U2b of DLLT-EM01 circuit d will be used in this section.

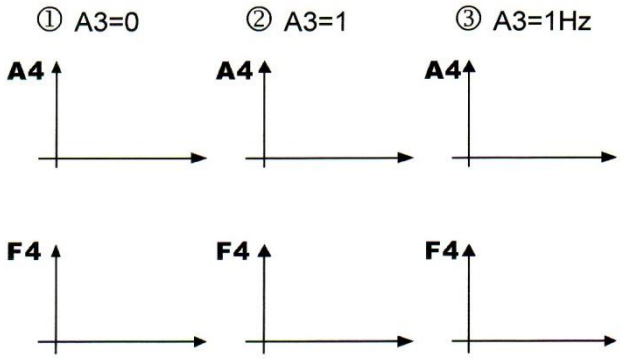
2. Connect inputs A3, A4 to SW0, SW1 TTL level and output F4 to L1. Follow the input sequences below and record output F.

STATE	INPUT		OUTPUT
	A4	A3	F4
0	0	0	
1	0	1	
2	1	0	
3	1	1	





3. Connect A4 to the 10Hz TTL level output of Clock Generator. Measure and record the input and output waveforms.



(c) INVERTER Gate Characteristics Measurement (Module DLLT-EM01 circuit d)

1. U3c of DLLT-EM01 circuit d will be used in this section.

2. Connect input C1 and output F6 of U3c to SW0 and L1 (LED) respectively. Follow the input sequences below and record outputs.

	C1	F6
0	0	
1	1	

1. Connect F6 to C2 with a test lead. Connect output F7 to L2 (LED). Follow the input sequences below and record the outputs.

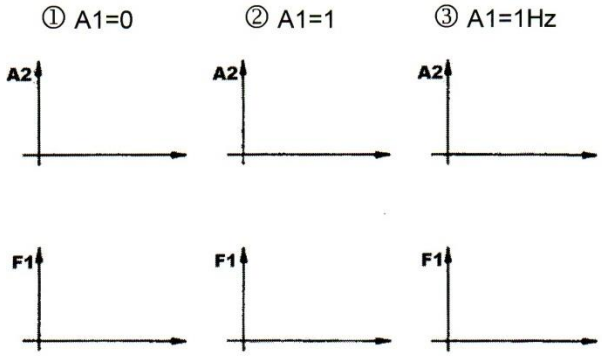
	C2	F7
0	0	
1	1	

(d) NAND Gate Characteristics Measurement (DLLT-EM01 circuit d)

1. U1a of DLLT-EM01 circuit d will be used in this section. Connect inputs A1, A2 to SW0, SW1 TTL level and output F1 to L1 (LED). Follow the input sequences below and record the outputs.

	A2	A1	F1
0	0	0	
1	0	1	
2	1	0	
3	1	1	

2. Connect 10Hz TTL level square wave to A2, measure and record input/output waveforms at the following conditions.

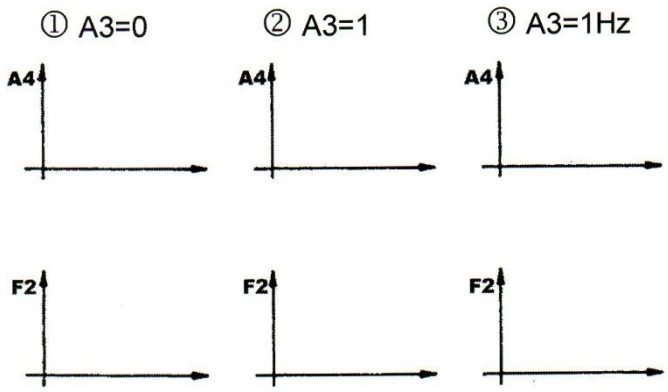


e) NOR Gate Characteristics Measurement (DLLT-EM01 circuit d)

1. U2a of DLLT-EM01 circuit d will be used in this section. Connect inputs A3, A4 to SW0, SW1 TTL level and output F2 to L1 (LED) Follow the input sequences below and record the outputs.

	A4	A3	F2
0	0	0	
1	0	1	
2	1	0	
3	1	1	

2. Connect TTL level 10Hz square wave to A4, observe and record input/output waveforms under the following conditions with an oscilloscope:

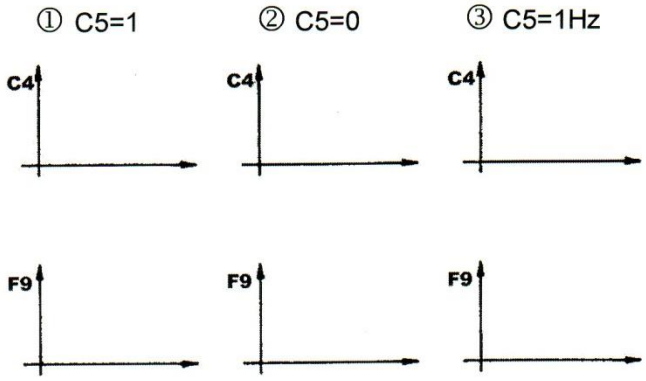


(f) XOR Gate Characteristics Measurement (DLLT-EM01 circuit d)

1. U4a of DLLT-EM01 circuit d will be used in this section. Connect inputs C4, C5 to SW0, SW1 TTL level and output F9 to L1 (LED). Follow the input sequences below and record the outputs.

	C5	C4	F9
0	0	0	
1	0	1	
2	1	0	
3	1	1	

2. Connect TTL level 10Hz square wave to C4, observe and record input/ output waveforms under the following conditions with an oscilloscope.



RESULTS

1. Phase relationship between input and output waveforms should be compared when square waves are added.

FAULT SIMULATIONS

Utilizing U1, U2, U5, U6

1. The high state voltage F1 should be approximately 4.4V when there are no loads. Measure U1a. Connect inputs A1, A2 and measure F1 again. Determine possible faults.

2. Input states of A1. A2, B1. Connect F3 to L1 and the output remains "1". Determine possible faults.

3. Input states of A3. A4, B2. Connect F4 to L2 and the output remains "0". Determine possible faults.

1-7 Interface between Logic Gates

OBJECTIVE

Understand the techniques of interface connection.

DISCUSSIONS

TTL and CMOS are the most often-used logic gates. Their specifications are shown below in Fig. 1-7 (a) and Table 1-7.

		TTL	COMS
SUPPLY VOLTAG		+5V±0.25V	3~18V
LOW INPUT VOLTAGE	Vil	≦0.8V	≦1.5V
HIGH INPUT VOLTAGE	Vih	≧2.0V	≧3.5V
LOW OUTPUT VOLTAGE	Vol	≦0.4V	0V
HIGH OUTPUT VOLTAGE	Voh	≧2.4V	5V
LOW INPUT CURRENT	Iil	≦1.6mA	≦0.1μA
HIGH INPUT CURENT	Iih	≦40μA	≦0.1mA
LOW OUTPUT CURRENT	Iol	≧16mA	≧1mA
HIGH OUTPUT CURRENT	Ioh	≧0.4μA	≧0.1mA

Table 1-7

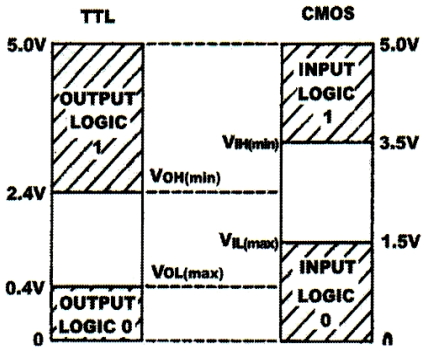


Fig. 1-7 (a)

From Table 1-7 we can see that CMOS gate's input voltage requirement is higher than TTL gate's output voltage capability.

If a TTL gate is used to drive a CMOS gate, TTL's output voltage must be increased to meet the input voltage requirement of CMOS. On the other hand, when CMOS is used to drive TTL the output current OF CMOS must be increased. This is why we must carefully review the date books before constructing any interface circuit.

A resistor Rx connected to the supply voltage can be added to increase the input voltage into CMOS when it is driven by TTL , as shown in Fig. 1-7 (B0 .The range of RX is 390Ω ~ 4.7KΩ for stranded series TTL and 820Ω ~ 12KΩ for LS series TTL.

When TTL is driven by CMOS a buffer should be added in between to increase the output current of CMOS. Two standard CMOS connected in parallel could drive a LS series TTL.

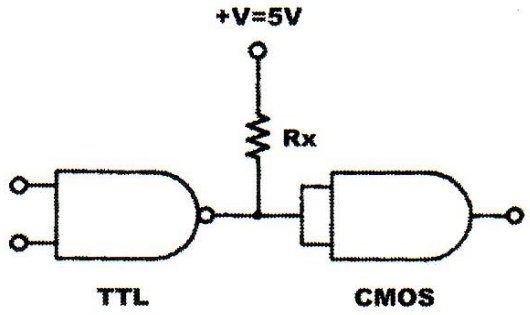


Fig. 1-7 (b)

EQUIPMENTS REQUJIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM01: Basic Logic Gates Experiment Module, Multimeter

EXERCISE

(a) TTL to CMOS interface (DLLT-EM01 circuit d/e)

1. Insert connection clips according to Fig. 1-7 (c). U1a is Standard series TTL gate which be used in this section of the experiment.

2. Using the Multimeter, adjust resistance of R14 to 2.2KΩ.

3. Connect output of F1 to input of U5a. Use +5V supply voltage for both TTL and CMOS gates. Connect input A1 to TTL output of Date Switch SW0. Measure and record voltages at A1; F1; A5 and Y1

A1	F1	A5	Y1
0			
1			

4. Connect F1 to R13, Vcc to R14 with connection clips. Again measure and record A1; F1; A5; and Y1 below.

A1	F1	A5	Y1
0			
1			

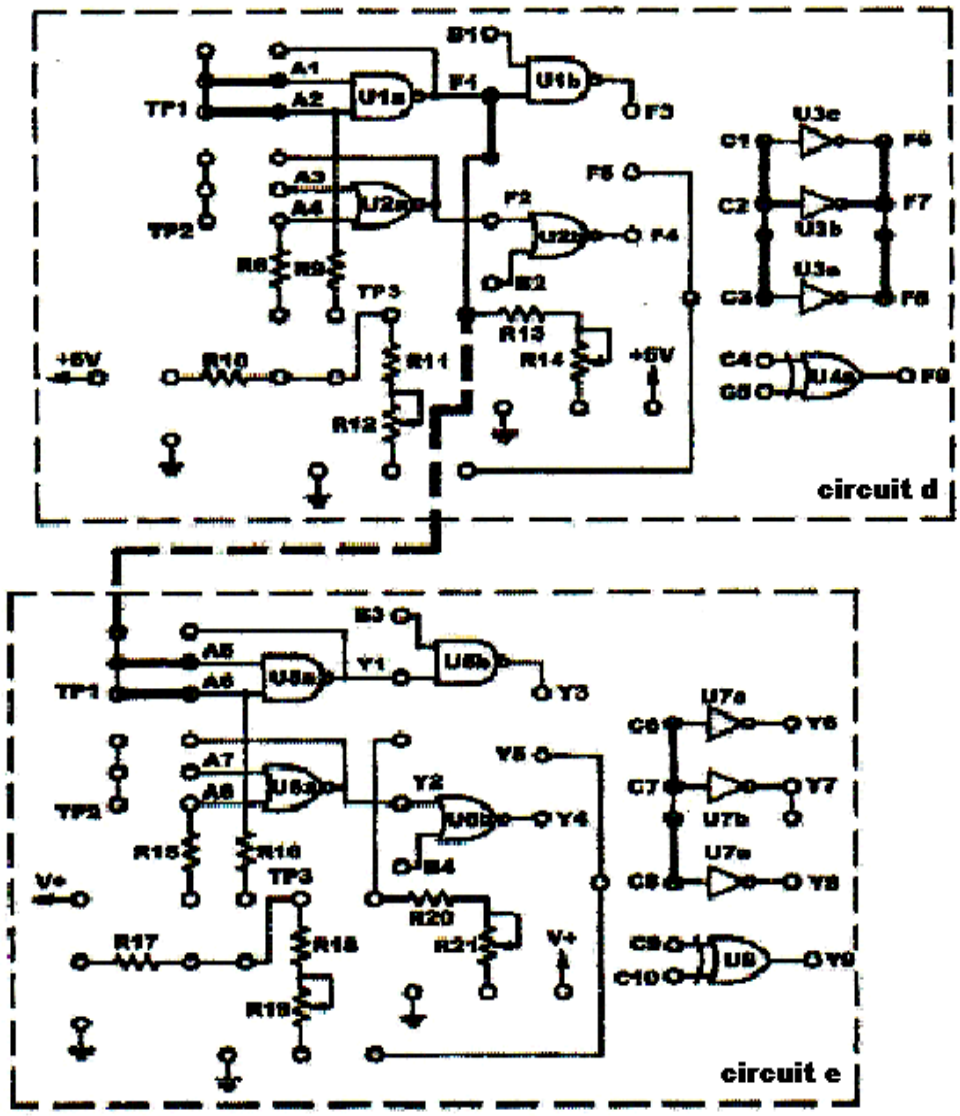


Fig. 1-7 (c)

(b) CMOS to TTL interface (DLLT-EM01 circuit d/e)

1. U7a~U7c on circuit e of Module DLLT-EM01 will be used in this section. Insert connection clips according to Fig. 1-7 (c).

2. Connect output Y8 of U7a to input A1 of U1a and C8 to Data Switch SW1 TTL level output. Measure and record Y8; A1; F1.

C8	Y8	A1	F1
0			
1			

3. Connection clips inserted between C6~C7, C7~C8 will connect C6~C7~C8 in parallel. Repeat the measurements.

C8	Y8	A1	F1
0			
1			

4. Connect Y8 to input C1, C2, C3 of U3a~ U3c. C1~C2~C3 as well as F6~F7~F8 are connected in parallel. Repeat the measurements.

C8	Y8	C1	F6
0			
1			

RESULTS

1. The theoretical high output voltage (Voh) of TTL is 2.4V, which is the minimum allowable voltage. However in actual applications of TTL to CMOS interface, the output voltage of TTL is close to +5V, enough to drive CMOS.

2. The addition of a resistor to the output of a TTL gate will increase its output voltage, as well as its tolerance to noise interference.

3. When the output state of CMOS is "1", its minimal output voltage is roughly 4.4V. On the other hand, the minimal input voltage requirement of TTL is about 2V so there is 2.4V of noise interference immunity or tolerance.

4. Can a CMOS gate drive a standard TTL gate? How about a LS series TTL gate?

DLLT-EM02 COMBINATIONAL LOGIC CIRCUITS

2-1 NOR Gate Circuit

2-2 NAND Gate Circuit

2-3 XOR Gate Circuit
- a. Constructing XOR Gate with NAND Gate
- b. Constructing XOR Gate with Basic Gate

2-4 AND-OR-INVERTER (A-O-1) Gate Circuit

2-5 Comparator Circuit
- a. Comparator Constructed with Basic Logic Gates
- b. Comparator Constructed with TTL IC

2-6 Schmitt Gate Circuit

2-7 Open-Collector Gate Circuit
- a. High Voltage/Current Circuit
- b. Constructing an AND Gate with Open-Collector Gate

COMBINATIONAL LOGIC CIRCUITS EXPERIMENTS

Combinational logic circuits are constructed with basic logic gates. Its output will correspond only to the current input, previous inputs and outputs can't influence the current output. Therefore the output of any combinational logic circuits can be expressed by Boolean functions.

The major component of a combinational logic circuit includes Input Variables; Logic Gates and Output Variables. The input variable could be either higher or lower than the output variable but both are binary signals, or "0" and "1".

Assuming there are "n" input variables, there will be 2 possible input combinations, each with one corresponding output combination. Before designing and constructing a combinational logic circuit the following information should be taken into consideration:

1. Truth tables of logic gates
2. Boolean Function
3. Karnaugh Map
4. de Morgan's Theorem

The following combinational logic gates are used very often and they are discussed in this chapter, along with many other combinational logic gates.

1. Combinational logic circuits with NAND and NOR gates
2. AND-OR-INVERTER (A-O-I) gate
3. XOR gate
4. Open-collector gates
5. Tristate gate
6. Arithmetic circuits
7. Encoder and decoder circuits

8. Multiplexer and demultiplexer circuits
9. Comparator circuits

2-1 NOR Gate Circuit

OBJECTIVE

Understanding how to construct other combinational logic gates using NOR gates.

DISCUSSION

The symbol of a NOR gate is shown in Fig. 2-1. The Boolean expression for the N gate is F= A + B; in de Morgan's theorem, F= A + B = A x B.

When A=B, F= A + B = A +A= A. When B=O, F= A + B = A + 0 = A. Therefore, the NOR gate can be used to construct NOT, OR; AND; NAND; and XOR gates. We will not attempt to construct various logic gates in this experiment by connecting NOR gates in different ways.

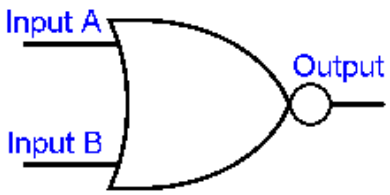


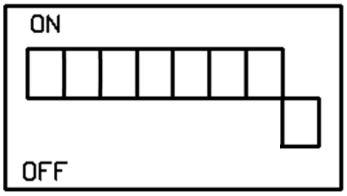
Fig. 2-1 Symbol of NOR gate

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM02

EXERCISE

7. Make sure the Fault Simulator DIP Switch follows the below setting :
8.



9. U1a of Fig. 2-2 (a) will be used to construct a NOT gate.

10. Connect inputs A, B to Data Switches SWO, SW1 and output F1 to Logic Indicator L1. Set SWO to "0", observe states of F1 at SW1="0" and SW1="1 ".
    Does the circuit act as a NOT gate? (As in Fig. 2-2 (b))

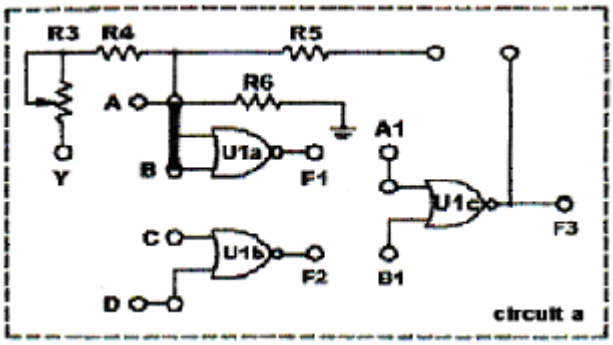


Fig. 2-2 (a) DLLT-EM02: Assembly Logic Circuits (1)

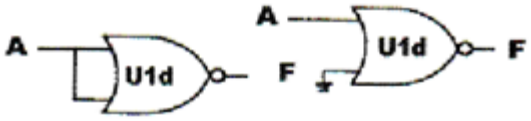


Fig. 2-2 (b) NOR gate used as NOT gate

11. Insert a connection clip between A and B. Connect A to SWO and F1 to L1. What is the state of F1 when SW0=0 and SW0=1?
    Does the circuit act as a NOT gate?

12. Use U 1a and U 1c to construct a buffer shown on the left side of Fig. 2-2 (c). Insert connection clips between A~ B; F1~A1; A1~ B1. Connect input A to SWO and output F3 to L1. What is the state of F3 when SW0=0 and SW0=1?
    Does the circuit act as a buffer?

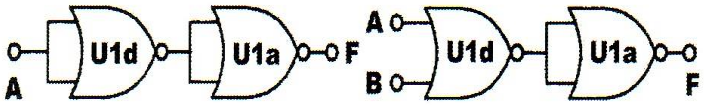


Fig. 2-2 (c) NOR gate use as Buffer and OR gate

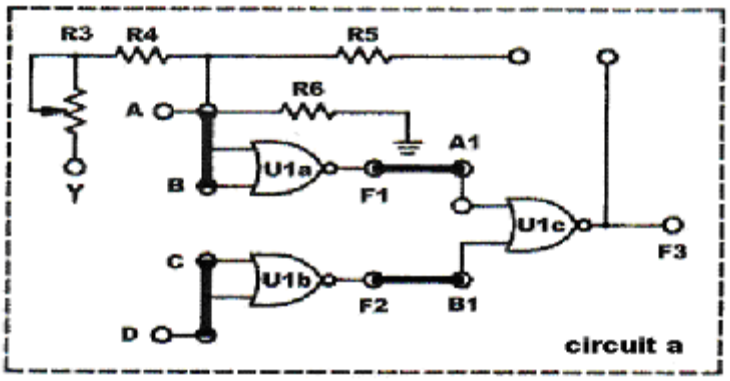
13. Use U1a and U1c to construct an OR gate shown on the right side of Fig. 2-2 (c). Insert connection clips between F1 ~A1 and A1~B1. Connect inputs A to SW0, B to SW1; and output F3 to L1. Follow the input sequences shown below and record the output states in Table 2-1.

SW1(B)	SW0(A)	F
0	0	
0	1	
1	0	
1	1	

Table 2-1

14. Insert connection clips according to the figure below. The circuit will act as an AND gate.

    (1) Connect A to SW0; D to SW1; F1 to Al; F2 to 131 - F3 to 1-1.
    (2) Follow the input sequences given below. Record the output states in Table 2-2.



SW1(D)	SW0(A)	F3
0	0	
0	1	
1	0	
1	1	

Table 2-2

RESULTS

1. NOR gate can be used to construct just about any basic logic gate.

2. There are two ways to use NOR gate as an inverter. Since TTL gates have higher current when the input is grounded, if TTL NOR gate is to be used as an inverter, its two inputs should be connected together.

FAULT SIMULATION

1. U1a and U1c are used as a buffer and the outputs stay in high state. Try to locate all possible faults.

2. The outputs stay at low state when U1a and U1c are used as a buffer. Try to locate all possible faults.

3. When U1a. U1b. U1c are used as an AND gate, the output F is only affected by the input A What could be the faults?

2-2 NAND Gate Circuit

OBJECTIVE

To understanding how the construct various combinational logic gates with NAND gates.

DISCUSSION

The symbol of a NAND gate is shown in Fig. 2-4. The Boolean expression for a NAND gate is F= $\overline{A \times B}$; in de Morgan's theorem, $\overline{A \times B}$ = A + $\bar{B}$.

When A=B, F= $\overline{A \times B}$ = A. When B=1, F= $\overline{A \times B}$ = $\overline{A \times 1}$ = $\bar{A}$. Like the NOR gates, NAND gates can be used to construct just about any basic logic gates. We will attempt to construct various basic gates in this experiment by connecting NAND gates in different ways.

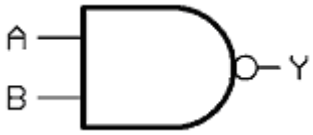


Fig. 2-4 Symbol of NAND gate

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM02: Assembled Logic Circuits (1) Experiment Module

EXERCISE

1. Insert connection clips according to Fig. 2-5(a), using U2c and U2d to construct the NOT gate shown on left side of Fig. 2-5(b).

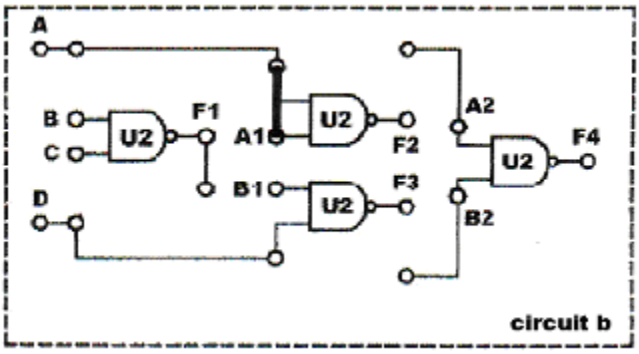
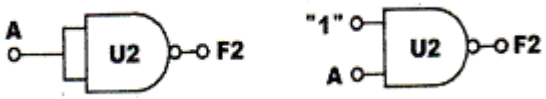


Fig. 2-5 (a)



(b) NOT gate constructed with NAND gate

(1) Connect input A to Data Switch SW1 and output F2 to A2 and Logic Indicator L1; connect 131 to Vcc ("1 "). Observe the output states.
When SW1="0", F2= _____
When SW1="1 ", F2= _____
Does the circuit act as a NOT gate?
(2) Connect input A1 to Vcc ("1 ") and remove the connection clip between A and A1 to create the NOT gate shown on the right side of Fig. 2-5 (b). Other connections remain the same. Observe the output states.

When SW1="0", F2= _____
When SW1="1", F2= _____
Does the circuit act as a NOT gate?

(3) Remove connection clips and insert them again according to Fig. 2-6 (a) to construct the AND gate shown in Fig. 2-6 (b). Connect A to SW1, A1 to SW2 and F4 to L1. Follow the input sequences given below and record the outputs in Table 2-4.

Does the circuit act as an AND gate (F=AxB)?

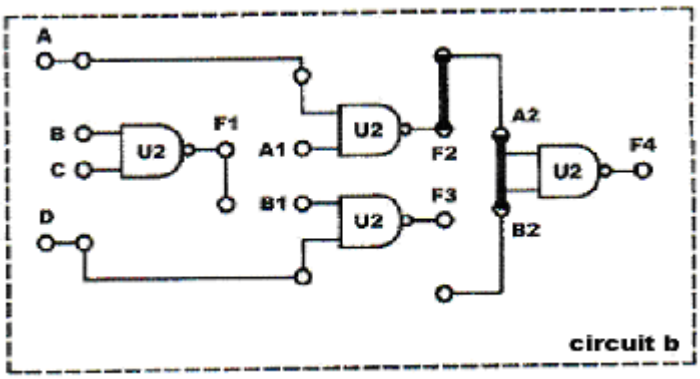


Fig. 2-6 (a)

SW2(A1)	SW1(A)	F4
0	0	
0	1	
1	0	
1	1	

Table 2-4

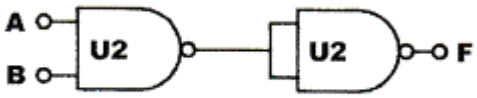


Fig. 2-6 (b)

2. Insert connection clips according to Fig. 2-7 (a) to construct the circuit of Fig. 2-7 (b). Connect A to A1 and SW1; F2 to A2; D to 131 and SW2; F3 to 132; F to 1-1. Follow the input sequences in Table 2-5 and record the outputs.

   Does the circuit act as an OR gate (F=A+B)?

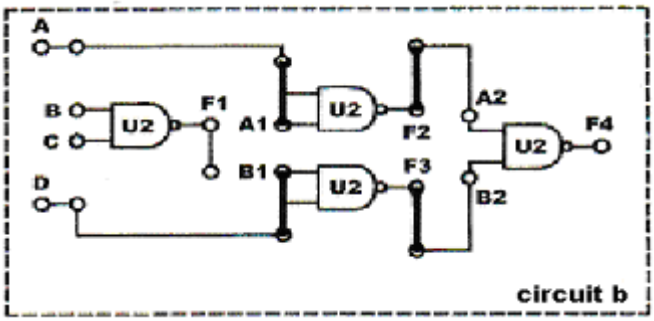
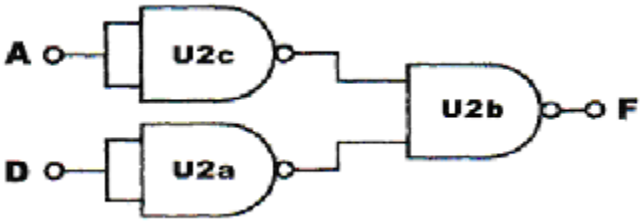


Fig 2.7 (a)



(b) OR gate constructed with NAND gate

SW2(D)	SW1(A)	F4
0	0	
0	1	
1	0	
1	1	

Table 2-5

RESULTS

1. NAND gates can be used to construct any basic logic gate.

2. There are two ways to construct inverters with NAND gates. Since the high state of TTL consumes almost no current, if NAND gates are used to construct inverters the spare input should be connected to high potential.

FAULT SIMULATION

1. The output F2 remains in low state when U2b is used to construct a NOT gate. What could be the faults?

2. When U2b, U2c, U2d are used to construct an OR gate, the output F remains in high state. What could be the faults?

2-3 XOR Gate Circuit

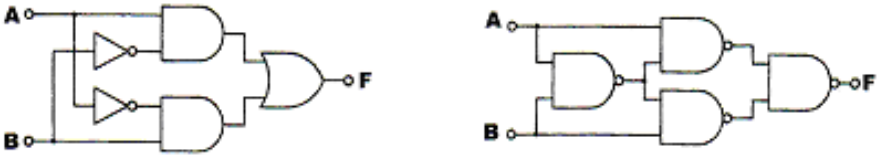
OBJECTIVE

Understand the characteristics of XOR gates.

DISCUSSION

The symbol of a XOR gate is shown in Fig. 2-8. The output F is equal to $\overline{A \oplus B} = \bar{A}B + A\bar{B}$. XOR gates can be constructed using NOT, OR, AND, NOR or NAND gates or by using four NAND gates, as shown in Fig. 2-9 (a) and (b).

Fig. 2-8 Symbol of XOR gate



(a) with basic gates (b) with NAND gates only

Fig. 2-9 XOR gate circuits

Since F= $\bar{A}$B+A $\bar{B}$, when B=0 F= $\bar{A}$ x 0+Ax 0=Ax1=1 and the circuit act as buffer. When B=1, F = $\bar{A}$ x 1 + A x $\bar{1}$ = $\bar{A}$ x 1= $\bar{A}$, the circuit act as an inverter. In other words, the input state of a XOR gate determines whether it will act as a buffer or an inverter. In this experiment, we will use basic logic gates to construct XOR gates and study the relationship between the inputs and outputs.

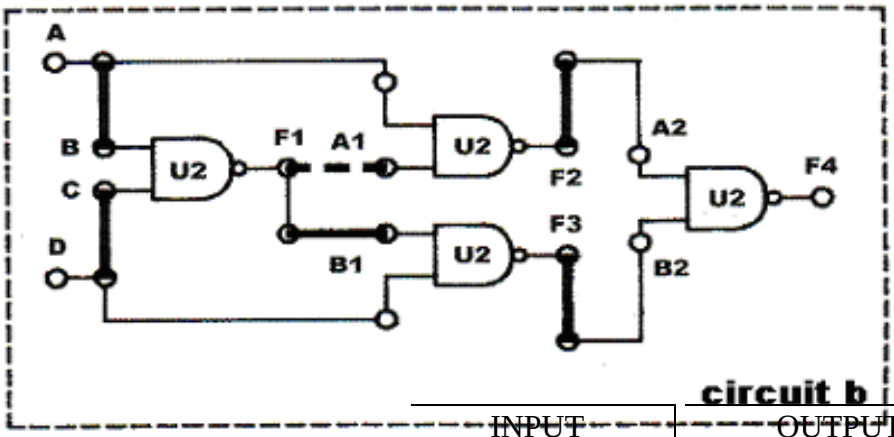
EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, DLLT-EM02: Assembled Logic Circuits (1) Experiment Module

EXERCISE

(a) Constructing XOR gate with NAND gate (Module DLLT-EM02 circuit b)

1. Insert connection clips according to Fig. 2-10 (a) to construct the circuit of Fig. 2-10 (b). Connect inputs A to SW1, D to SW2; outputs F1 to L1, F2 to L2; F3 to L3 and F4 to L4.



INPUT		OUTPUT			
SW2(D)	SW1(A)	F1	F2	F3	F4
0	0				
0	1				
1	0				
1	1				

Fig 2.10 (a)

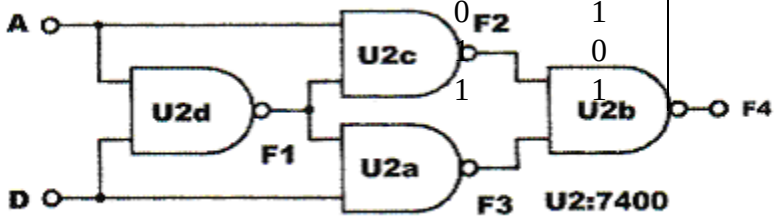


Fig 2.10 (b) equivalent circuits

2. Follow the input sequences for A and D in Table 2-6 and record the outputs.

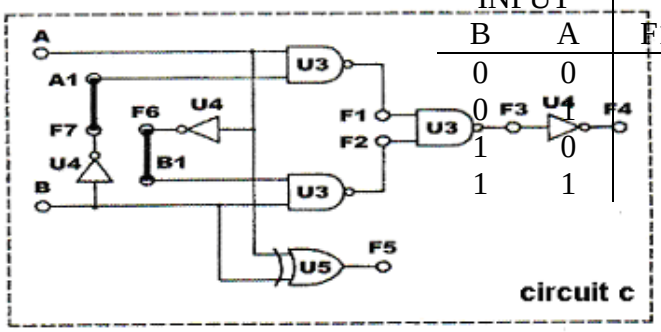
3. Determine the Boolean expression for F1, F2, F3, F4.

(b) Constructing XOR Gate with Basic Gate (DLLT-EM02 circuit c)

1. Insert connection clips according to Fig. 2-11 (a) to construct the equivalent circuit of Fig. 2-11(b).

2. Connect input A, B to SW1 SW2; outputs F1, F2, F3, to L1, L2, L3.

3. Follow the input sequences for A and B in Table 2-7 and record the output.



INPUT		OUTPUT			
B	A	F1	F2	F3	F4
0	0				
0	1				
1	0				
1	1				

Fig 2.11 (a)

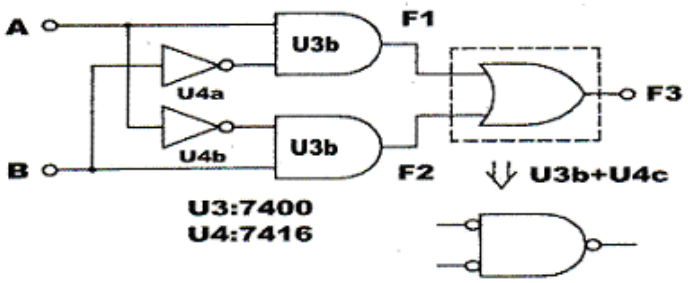


Fig 2.11 (b) equivalent circuits

Table 2-7

1. Can this work as an XOR gate? If not how to modify it?

RESULTS

1. XOR gate can be constructed with either basic gates or four NAND gates with the same results. However, using four NAND gates is much simpler.

2. By adding a NOT gate to the output of a XOR gate it can be converted into an XNOR.

FAULT SIMULATIONS

1. What could be wrong if 4 NAND gates are used to construct a XOR gate and the output F=D?

2. What could cause the output F3 of a XOR gate made with basic gates to remain in high state?

2-4 AND-OR-INVERTER (A-O-I) Gate Circuits

OBJECTIVE

Understand the basic principled of combined logic.

DISCUSSION

AND-OR-INVERTER (A-O-I) gates consist of two AND gates, one OR gate and one INVERTER (NOT) gate. The symbol of an A-O-I gate is shown in Fig. 2-12. The Boolean expression for the output F is

F= $\overline{AB+CD}$ ..... Equation (1)

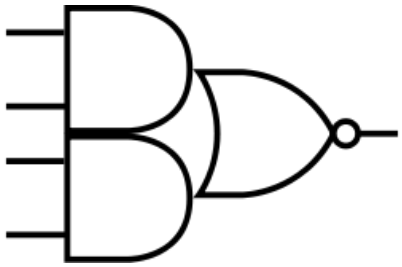


Fig. 2-12

Equation (1) can be converted into de Morgan's theorem as:

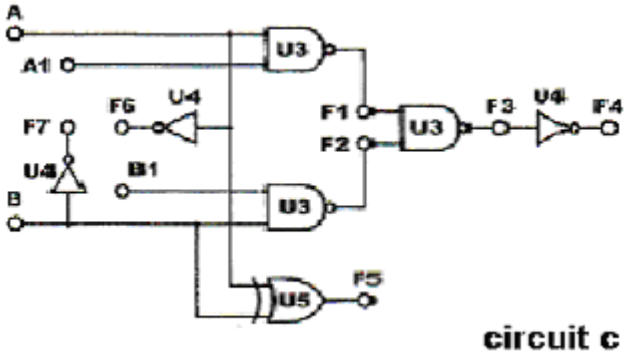
F= ($\bar{A}+\bar{B}$) x ($\bar{C}+\bar{D}$)..... Equation (2)

Equation (1) is also referred to as "Sum of Products".
Equation (2) is also referred to as "Product of Sum".
Basically, the A-O-I gate is a "Sum of Products" logic combination.

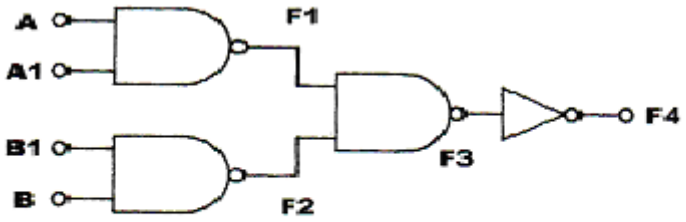
EQUIPMENTS REQUIRED
DLLT-1300 Digital Logic Lab Trainer; DLLT-EM02: Assembled Logic Circuits (1) Experiment Module

EXERCISE

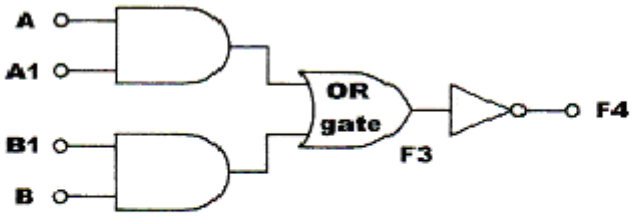
1 Use U3a, U3b, U3c and U4c on block c of DLLT-EM02, shown in Fig. 2-13 (a), to construct the A-O-I gate of Fig. (b). Fig. 2-13 (c) is the equivalent A-O-I circuit which uses U3a, U3b, U3c used as the OR gate.



(a)



(b) actual circuit



(c) eq uivalent circuit

Fig. 2-13-A-O-I circuit

2. Connect inputs A, A1, B, 131 to Data Switches SW0, SW1, SW2, SW3 respectively. Connect outputs F3, F4 to Logic Indicators L1 and L2.

3. Set BxB1 to "0", follow the input sequences for A, A1 in Table 2-8 and record the outputs.

BxB1 = 0

A1	A	F3	F4
0	0		
0	1		
1	0		
1	1		

Table 2-8

Does F3 act as an AND gate between A and A1?

4. When BxB1 ≠ 0, Does F3 act as an AND gate between A and A1? (F3=AxA1)

5. When A=A1=0, follow the input sequences for B, 131 in Table 2-9 and record the outputs.

A1x A = 0

B1	B	F3	F4
0	0		
0	1		
1	0		

1	1

Table 2-9

Does F3 act as an AND gate between B and 131?

6. When AxA1≠ 0, Does F3 act as an AND gate between B and B1?

7. Does F3 equal to AxA1+BxB1?

RESULTS

1. A-O-I gate can also be constructed using two AND gates and one NOR gate.

2. The following TTL ICs has A-O-I function: 7450; 7451; 7453; 7454; 7460; 7464; 6465. Some of them are 2- input OR gates and some are multiple-input OR gates. Some has expanded input terminals or open output gates to enable logic combination capabilities.

FAULT SIMULATION

1. The output F4 remains in low state, regardless of the input states of A, A1, B, B1. What could be the problem?

2-5 Comparator Circuit

OBJECTIVE

Understand the construction and operational principles of digital comparators.

DISCUSSION

At least two numbers are required to perform any comparison. The simplest form of comparator has two inputs. If the two inputs are called A and B there are three possible outputs: A>B; A=B; A<B. Fig. 2-14 shows the schematic and symbol of a simple comparator.

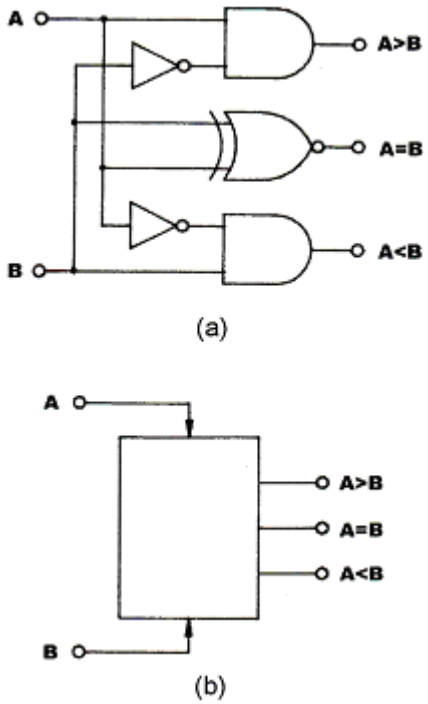
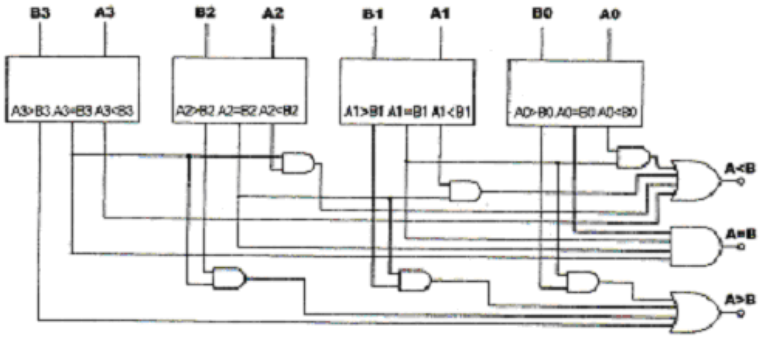


Fig. 2-14 Comparators

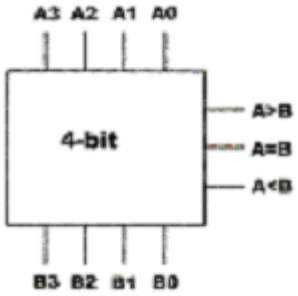
A 1-bit comparator is shown in Fig. 2-14. In actual applications 4-bit comparators are used most often. 4-bit comparator ICs that determine greater or less inputs include TTL 7485 and CMOS 4063. TTL 74689 is an IC that only compares whether the inputs are equal.

In a 4-bit comparators, each bit represents 2^0, 2^1, 2^2, 2^3. Comparisons will start from the highest bit (23), if input A is higher than input B at the 23 bit, the "A>B" output will be in high state.

If A and B are equal at the 2^3 bit, comparison will be carried out at the next highest bit 2^2. If there is still no result at this bit the process is repeated again at the next bit. At the lowest bit 2^0, if the inputs are still equal then the "A=B" output will be in high state.



Expansion of comparator



(a) Symbol of 4-bit comparator

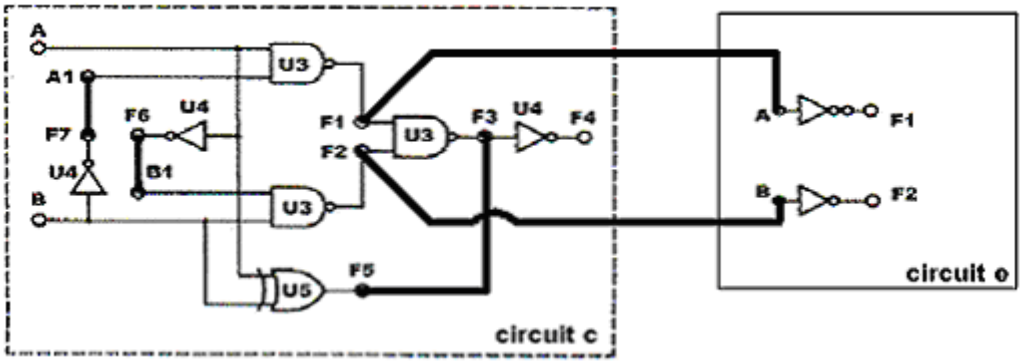
EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; Module DLLT-EM02: Assembled Logic Circuits (1) Experiment

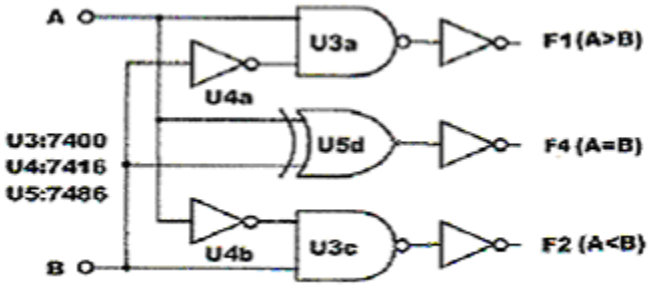
EXERCISE

(a) Comparator Constructed with Basic Logic Gates

1. Insert connection clips according to Fig. 2-16 (a). U3a, U3b, U3c, U4a, U4b, U4c and U5 will be used to construct the 1-bit comparator shown in Fig. 2-16 (b).



(a)



(b)

Fig. 2-16 1 bit comparator

2. The inputs are triggered by high state voltage. Connect inputs A and B to Data Switch SW1 and SW2. The outputs are triggered by low state voltage. Connect outputs F1, F2, F5 to Logic Indicators L1, L2. L3 respectively.

3. Follow the input sequences in Table 2-10. Measure and record the outputs.

INPUT			OUTPUT		
SW2(B)	SW1(A)		F1	F2	F5
0	0	A=B			
0	1	A>B			
1	0	A<B			
1	1	A=B			

Table 2.10

(b) Comparator Constructed with TTL IC

1. Circuit d of module DLLT-EM02 will be used in this section. U6 is a 7485 4-bit Comparator IC. Its pin assignment and truth table are given below.

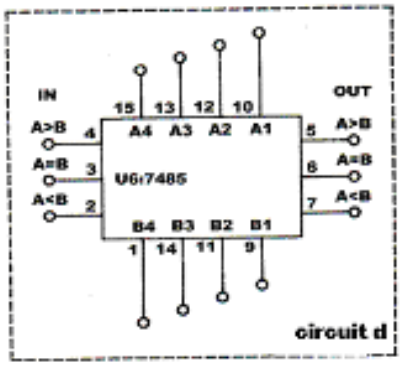
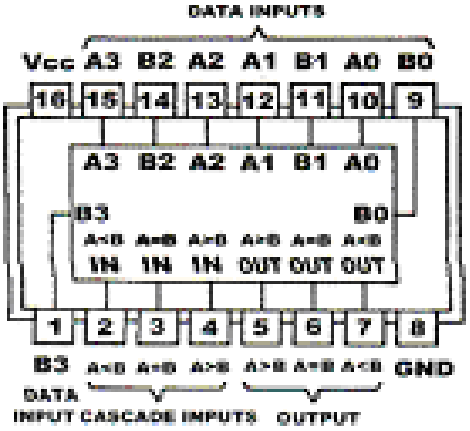


Fig 2-17



FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L

A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

2. Connect input A>B to SW1 and F1; A=B to SW2 and F2; A<B to SW3 and F3. Connect inputs A1~b A4 and B1~ B4 of the 7458 to the output of Thumbwheel Switches on DLLT-1300.

3. Assuming inputs A1 ~ A4=As and B1 ~ B4=Bs and As=Bs, follow input sequences in Table 2-11 and record the outputs.

INPUT			OUTPUT		
SW3	SW2	SW1			
A>B	A=B	A<B	A<B	A=B	A>B
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	1			

Table 2-11

4. Set SW3 to "0"; SW2 to "'I"; SW1 to "0". Observe and record the outputs under the following conditions:
   (1) As>Bs
   (2) As=Bs
   (3) As<Bs

5. Remove A1~ A4 and B1~ B4 from the Thumbwheel Switches and connect them to DIP Switches DIP1.0 ~ DIP1.3 and DIP2.0 ~ DIP 2.3 respectively. Repeat step 4. Are the results any different from step 4?

RESULTS

1. 1-bit comparator has three outputs: A>B; A=B; A<B

2. 7485 is a 4-bit comparator. Serial inputs A>B; A=B; A<B are the results of low bit comparisons. Serial inputs have no effect unless the high bits are equal.

FAULT SIMULATIONS

1. The 7485 is connected to the thumbwheel switch but the outputs are incorrect when Bs=2, 3, 6, 7.What could cause this problem?

2. What if Bs=4, 5, 6, 7 for the same circuit, will there be other causes?

2-6 Schmitt Gate Circuit

OBJECTIVE

Understand the structure and characteristics of Schmitt gates.

DISCUSSION

Schmitt gate is a unique logic gate with the following characteristics:

1. It will take in random input waveforms and transform them into uniform output waveforms The Schmitt gate is triggered only after the input voltage exceeds its positive threshold voltage VTH. It will change state again when the input voltage drops below the negative threshold voltage VTL.

2. VTH must be greater than VTL. The area between VTH and VTL is called "Hysteresis".

3. Since the Schmitt gate has VTH and VTL, it's less susceptible to noise interference which affects most logic gates. The output pulses of Schmitt gate have higher speed too. Fig. 2-18 (a) is a comparison of Schmitt gate input/output waveforms. Fig. 2-18 (b) demonstrates how a Schmitt gate can be constructer using basic logic gates.

   When Vo=0, Vs x $\frac{R2}{R1+R2}$ if Vs is large enough Vi will exceed VTH.

   When Vs exceeds VTH, Vo= Vcc and Vi= Vs x $\frac{R2}{R1+R2} + \frac{Vcc \times R1}{R1+R2}$, If Vs is small enough Vi will drop below VTL.

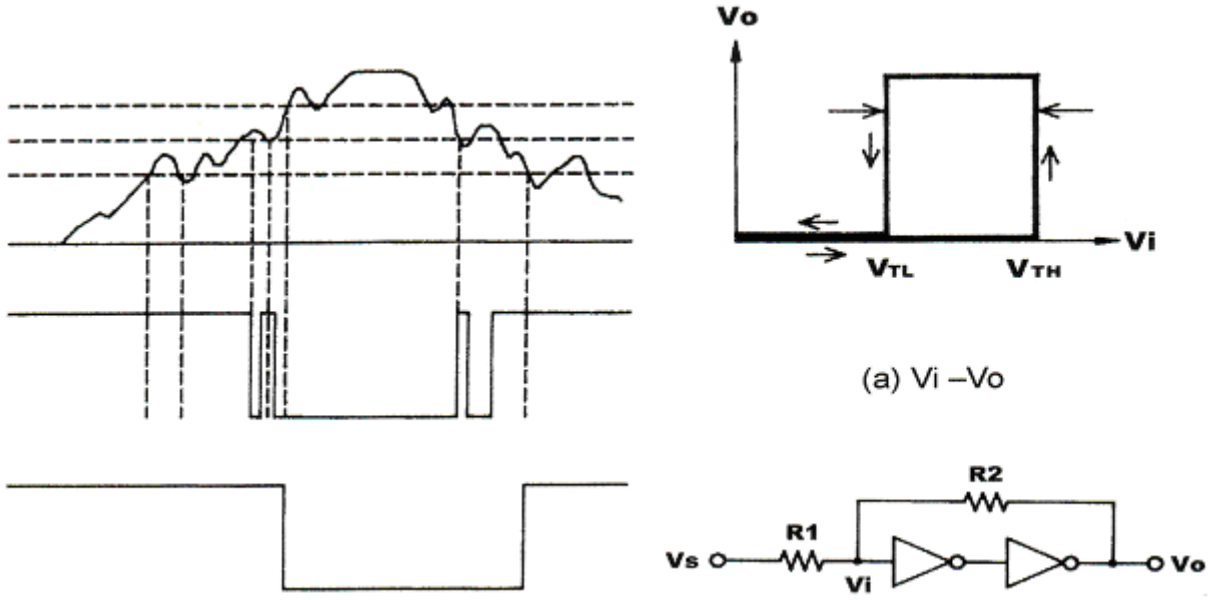


Fig. 2-18 Schmitt gate

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM02: Assembled Logic Circuits (1) Experiment Module.

EXERCISE

1. Insert connection clips according to Fig. 2-19 (a). Fig. 2-19 (b) is the equivalent circuit.

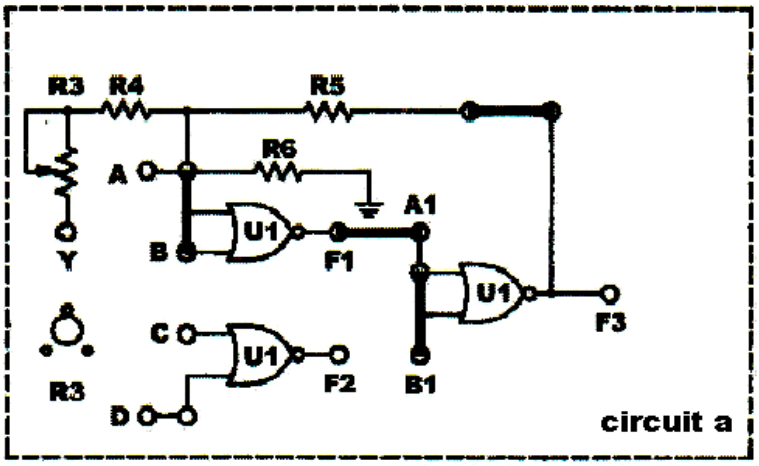


Fig. 2-19 (a)

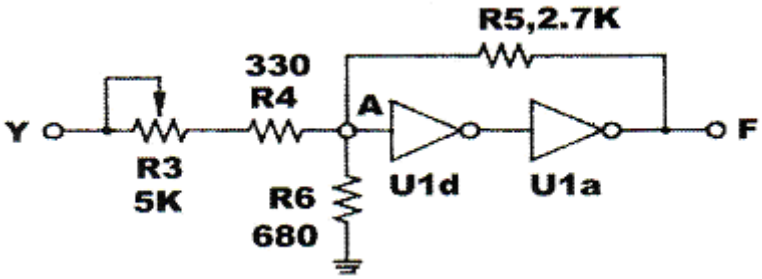


Fig. 2-19 (b)

2. Connect input Y to the sine wave output of Signal Generator. Adjust R3 to set the output F to square wave. Sketch the waveforms at point F (VF) and point A (VA) in Table 2-12.

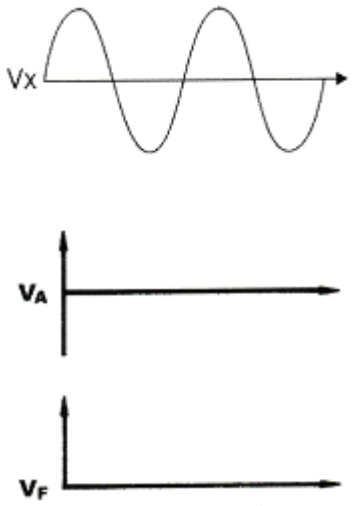


Table 2-12

RESULTS

1. The output of this circuit is high-speed pulses.

2. The input sine wave of Schmitt gates has two critical points: the Upper and Lower Trigger Point.

2-7 Open-Collector Gate Circuit

OBJECTIVE

Understanding the characteristics of open-collector gates and functions of wire-AND gates.

DISCUSSIONS

An Open-Collector gate, or O.C., is shown in Fig. 2-20 (a). The collector pole of Q3 must be open. If Y is to function, a load or resistor must be connected. The advantages of having the collector pole open are:

1. High voltage loads can be driven directly.

2. Wire-AND gates can be constructed.

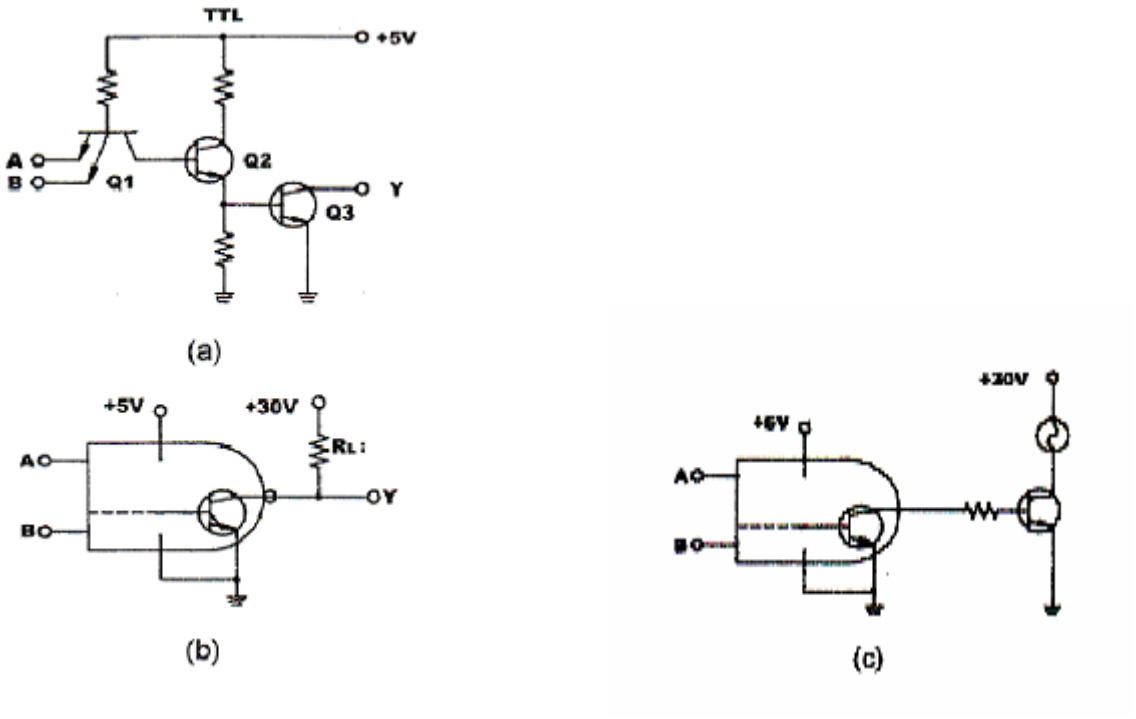


Fig. 2-20

(1) Directly Driven High Voltage Loads

Refer to Fig. 2-20 (b), the gate voltage is +5V and the load RL is connected to +30V. If larger loads, such as light bulbs or relays are to be driven, simply connect an additional transistor as shown in Fig. 2-20 (c).

(2) Wire-AND Gate

When the outputs of the NAND gate of Fig. 2-21 (a) is connected in parallel and one of the outputs is "0", the final output of the gate will be "0". In this case the NAND gate act as an AND gate. Logic gates such as this are called "wire-AND" gate.

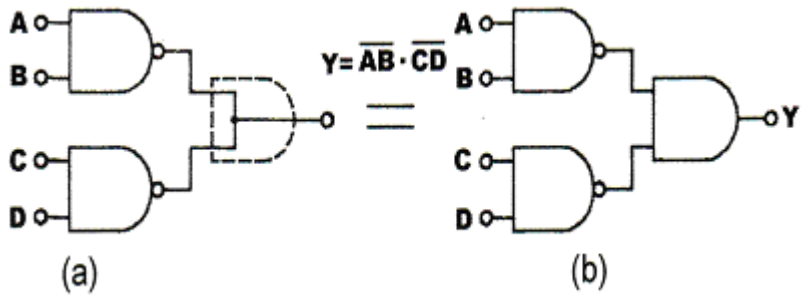


Fig.2-21 wire-AND gate

The equivalent circuit is shown in Fig. 2-21 (b).

Although logic gates can be combined to act as wire- AND gate, outputs of TTL gates should not be connected in parallel in order to prevent IC damages due to the high current generated when inputs of TTL IC are connected in parallel.

TTL ICs usually have tandem-type outputs. Refer to Fig. 2-22.

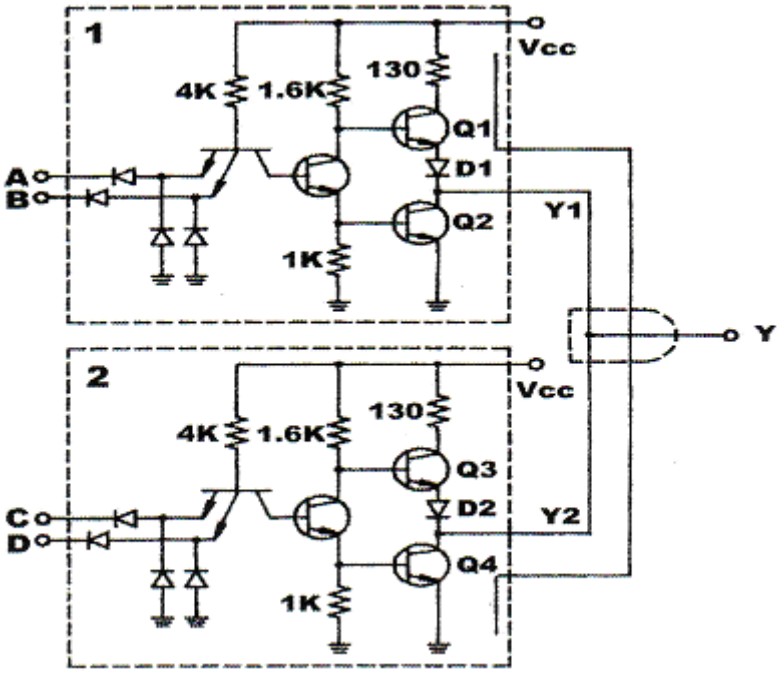


Fig. 2-22

If output Y1 is in high state and output Y2 is in low state, theoretically, Y (Y=Y1 xY2) should be in low state. At this point Q1 and Q4 are ON and Vcc passes through the 13052 resistor to Q1. D1 is grounded through Q4 and high current are generated and consumed by the IC internally. The high current is not the result of driving external loads. This is the why "tandem" type TTLs are not suitable for constructing wire- AND gates.

A typical open collector gate with connected outputs is shown Fig. 2-23.

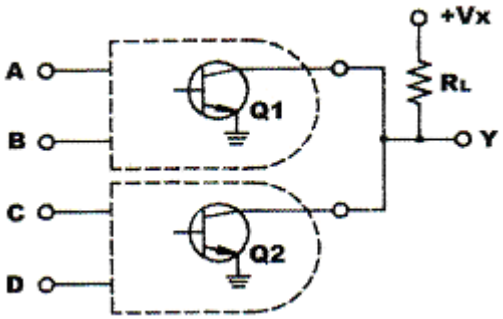


Fig. 2-23

Resistor RL is an external device. When RL is not connected, neither Q1 or Q2 will be on. If RL is connected and Q1 is on; Q2 is off, the external voltage +Vx will flow to Q1 through RL. Q2 has no current and the output Y=1. Reversely, if Q1 is off and Q2 is on, +Vx will flow to Q2 and Y=0. No large current are generated by the IC internally, since the current will pass through the load.

The wire-AND gate has very important applications. For example, a 4Kb memory can be expanded to 32Kb by using the wire- AND connection to connect eight 4Kb memories together.

TTL ICs with open collector function includes 7401, 7403, 7405, and 7409. The 7406 and 7407 have open collector as well as buffer/driver functions and can withstand voltages of 30V or higher. Refer to Fig. 2-24 for the circuit of a 7406.

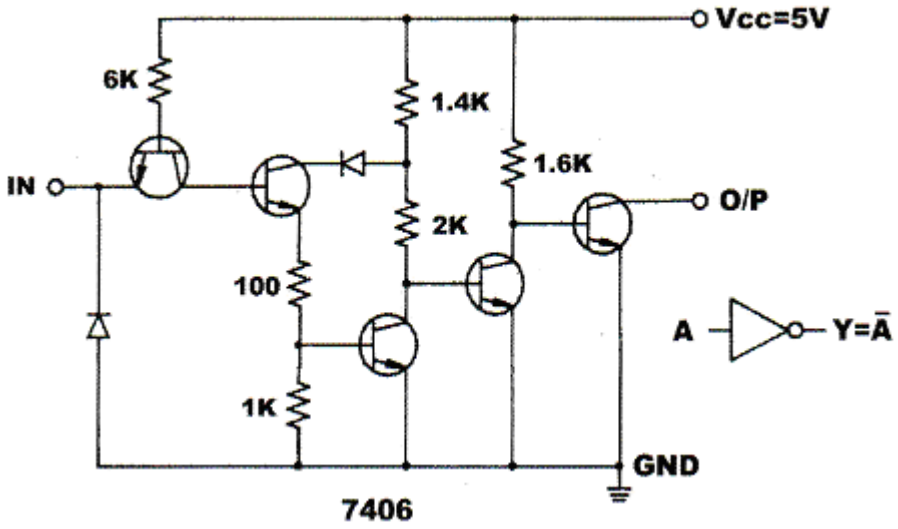


Fig. 2-24

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; Module DLLT-EM02: Assembled Logic Circuits (1) Experiment Module; Multimeter

EXERCISE

(a) High Voltage/Current Circuit

1. Connect C to +Vcc; input A to Data Switch SW1; output F1 to Logic Indicator L1. Measure the output voltage and observe L1 at A="0" and A="1 ".

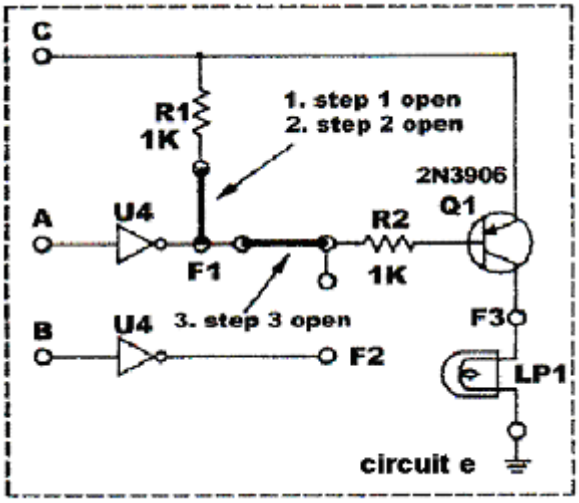


Fig. 2-25

(1) When A=O, F1= _____ V. What is the state of L1?
(2) When A=1, F1= _____ V. What is the state of L1?

2. Insert one connection clip between F1 and R1. Connect input C to the Adjustable Power Supply and set the output to its maximum value. A and F1 are still connected to SW1 and L1 respectively. Measure F1 and observe L1 at A=0 and A=1.

(1) When A=O, F1= _____ V. What is the state of L1?
(2) When A=1, F1= _____ V. What is the state of L1?

3. Remove the connection clip between F1 and R1. Insert it between F1 and R2 to use the light bulb as a load. Other connections remain the same. Observe the state of L1.

(1) When A=O, What is the state of L1?
(2) When A=1, what is the state of L1?

(b) Constructing an AND Gate with Open Collector Gate

1. Insert connection clips according to Fig. 2-26 (a). The equivalent circuit is shown in Fig. 2-26 (b). Connect inputs A, B to SW0, SW1; output F3 to L1. Measure F3 and observe L1.

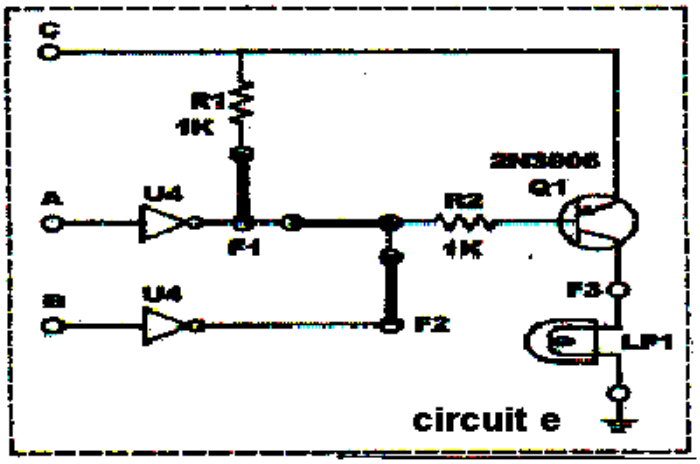


Fig. 2-26 (a)

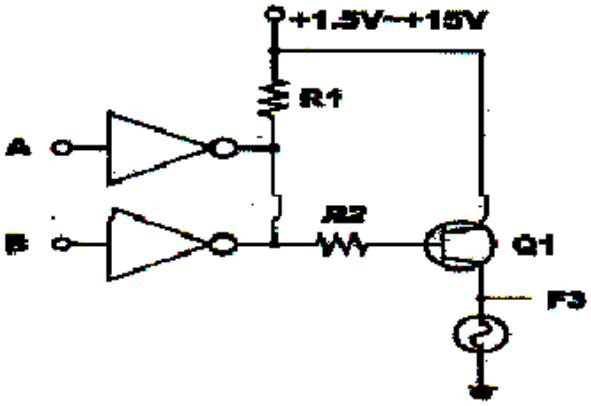


Fig. 2-26-(b)

2. When SW0 (A) = SW1 (B) =0, F3 = _____ V. L1 = _____ .
   When SW0 (A) = SW1 (B) = 1, F3 = _____ V .L1= _____.
   When SW0 (A) ≠ SW1 (B), F3 = _____ V .L1 = _____.

3. This circuit acts a _____ gate.

RESULTS

1. The open-collector gate will be in "open" state and have no logic functions without any external resistor or load.

2. The external resistor connected to an open-collector gate can be connected to any voltage as long as it is within the limitation of the circuit.

3. If outputs of a open-collector gate are connected in parallel it will serve act as an AND gate.

DLLT-EM03 COMBINATIONAL LOGIC CIRCUITS

3-1 Tristate Gate Circuit
- a. Truth Table Measurements
- b. Constructing an AND Gate with Tristate Gate
- c. Bidirectional Transmission Circuit

3-2 Half-Adder and Full-Adder Circuit
- a. High-Speed Adder Carry Generator Circuit

3-3 Arithmetic Logic Unit (ALU) Circuit

3-4 Bit Parity Generator Circuit
- a. Bit Parity Generator IC

COMBINATIONAL LOGIC CIRCUITS EXPERIMENTS

Combinational logic circuits are constructed with basic logic gates. Its output will correspond only to the current input, previous inputs and outputs can't influence the current output. Therefore the output of any combinational logic circuits can be expressed by Boolean functions.

The major component of a combinational logic circuit includes Input Variables; Logic Gates and Output Variables. The input variable could be either higher or lower than the output variable but both are binary signals, or "0" and "1".

Assuming there are "n" input variables, there will be 2 possible input combinations, each with one corresponding output combination. Before designing and constructing a combinational logic circuit the following information should be taken into consideration:

1. Truth tables of logic gates
2. Boolean Function
3. Karnaugh Map
4. de Morgan's Theorem

The following combinational logic gates are used very often and they are discussed in this chapter, along with many other combinational logic gates.

1. Combinational logic circuits with NAND and NOR gates
2. AND-OR-INVERTER (A-O-I) gate
3. XOR gate
4. Open-collector gates
5. Tristate gate
6. Arithmetic circuits
7. Encoder and decoder circuits
8. Multiplexer and demultiplexer circuits
9. Comparator circuits

3-1 Tristate Gate Circuit

OBJECTIVE

Understand the characteristics and applications of tristate gates.

DISCUSSIONS

Schematic and symbol of a tristate gate are shown in Fig. 2-27 (a) and (b) respectively. The structure of the tristate gate is basically the same as other logic gates, with the addition of a transistor Q5 and diodes D1, D2 for controlling the three states. The so-called "three states" are "0"; "1" and "X" for "open".

When the input for Q5's control terminal C is "1", Q5 is on, Q3 is grounded through D1 and Q5 so Q3 is off. If Q3 is off, Q2 and Q1 will also be off. The output F is "floating" since there are no high or low voltages.

The tristate gate will function properly when Q5 is off and C="0" because D1 and D2 can't be grounded through Q5. Q1, Q2 and Q3 will all be on and the gate will operate according to the states of inputs A and B. The output F will be either "0", or "1 ".

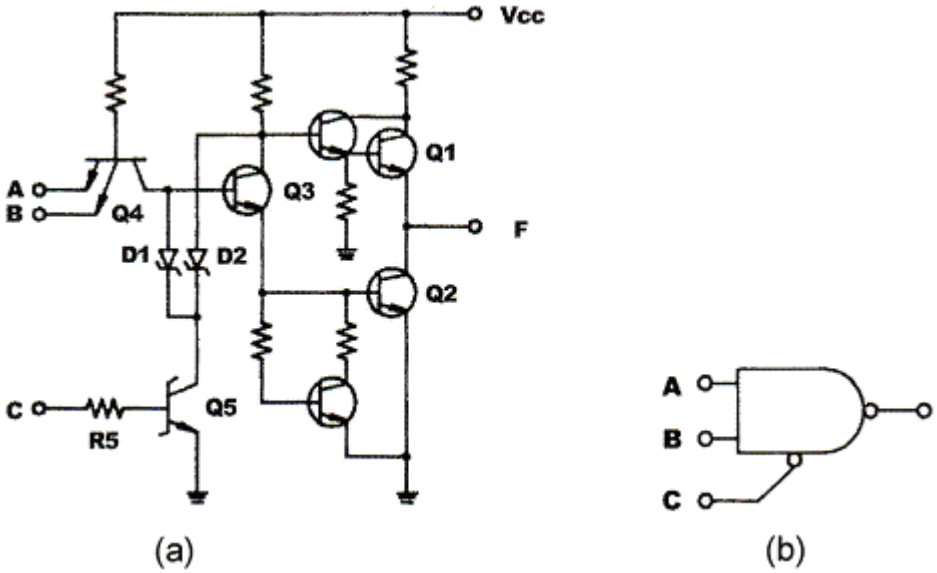


Fig. 2-27

The additional "open" state of tristate gates makes it ideal for data transmissions. Fig. 2-28 shows a bidirectional transmission scheme with tristate gates U1 and U2. U1 triggers on "1" and U2 triggers on "0".

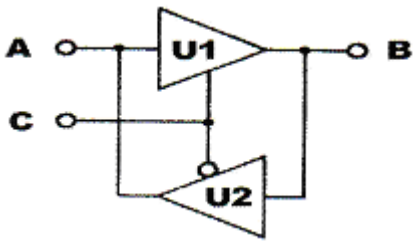


Fig. 2-28 Bidirectional data transmission

When C="1", U1 transmits data from A to B and U2 is open.

When C="0", U2 transmits data from B to A and U1 is open.

Tristate gates also can be connected in parallel but the down side to doing this is that only one gate can be triggered at a time. Short-circuit will result if more than one gate is triggered at a time. Fig. 2-29 shows parallel-connected tristate gates acting as a multiplexer.

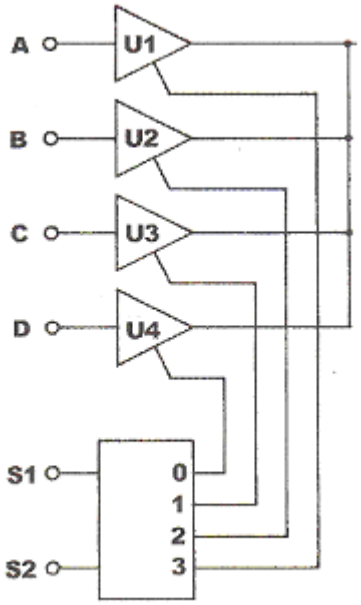


Fig. 2-29 Multiplexer constructed with tristate gates

Tristate gates are particularly useful in circuits with parallel outputs, such as memory expansion circuits and parallel control circuits.

A CMOS tristate gate is shown in Fig. 2-30. Its operating principles are described below.

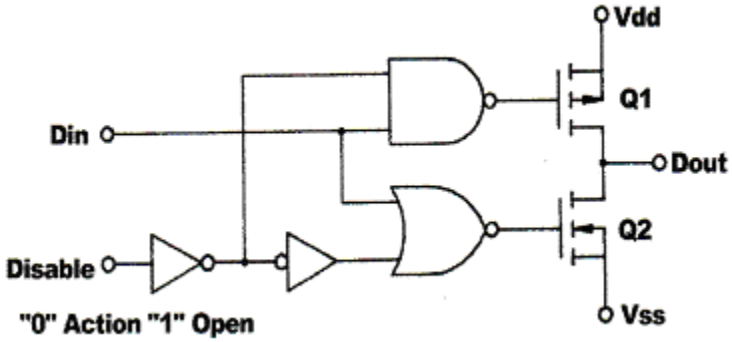


Fig. 2-30 CMOS tristate gate

(1) When DISABLE="0", the NOR and NAND gates are both control led by the input Din.
When Din="0", output of NAND gate is "1"; Q1 =off
When Din="0", output of NOR gate is I"; Q2=on; Dout="0"
When Din="1", output of NAND gate is "0"; Q1 =on

When Din="1", output of NOR gate is "0"; Q2=off; Dout="1"
Output Dout accepts data from input Din.

(2) When DISABLE="1 ", output of NOR gate will remain "0"; data at Din will not be send to the output of NOR and Q2 stays off; output of NAND remain "0". Data at Din will not influence the output so Q1 will remain off. Since both Q1 and Q2 are off, output Dout will be floating.

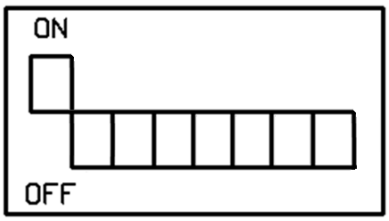
EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM03: Assembled Logic Circuits (2) Experiment Module, and Digital Multimeter

EXERCISE

(a) Truth Table Measurements

1. Make sure the Fault Simulator DIP Switch follows the below setting :
2.



3. U5a on circuit c of Module DLLT-EM03 will be measured in this section of the experiment.

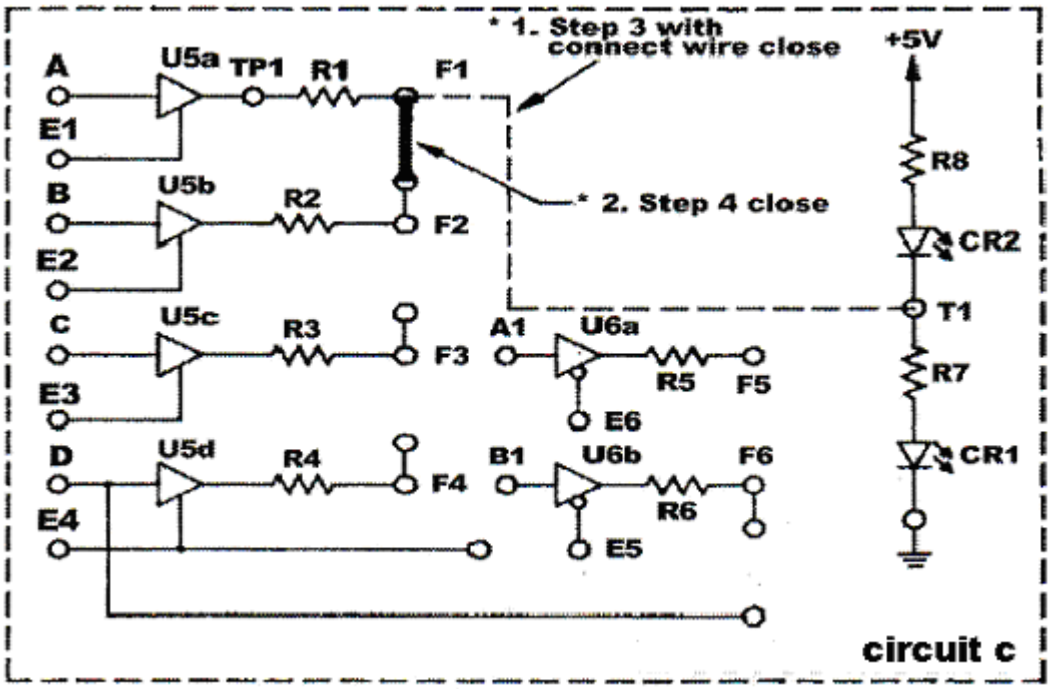


Fig. 2-31 of DLLT-EM 03‘s circuit c

4. Connect inputs A, E1 to Data Switches SW0, SW1.Follow input sequences in Table 2-13, measure and record the output F1 with a multimeter.

INPUT		OUT
SW1(E1)	SW0(A)	F
0	0	
0	1	
1	0	
1	1	

Table 2-13

5. Using a connection lead, connect F1 with T1 to construct the circuit of Fig. 2-32. Inputs A, E1 are still connected to SW0 and SW1. Follow the input sequences in Table 2-14, record output F1 and states of LEDs CR1, CR2. Record "1" if the LED is on and "0" if LED is off. (What happens if U6a is used instead?)

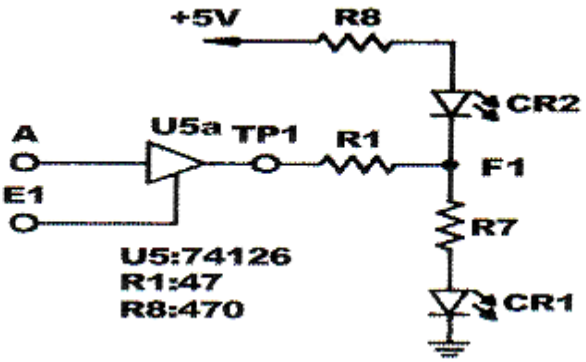


Fig. 2-32

INPUT		OUT		
SW1(E1)	SW0(A)	F1	CR1	CR2
0	0			
0	1			
1	0			
1	1			

Table 2-14

Notes: If CR1 and CR2 both are on, output F1 is open.

(b) Constructing an AND Gate with Tristate Gate

1. Construct the circuit shown in Fig. 2-33 on circuit c of Module DLLT-EM03.

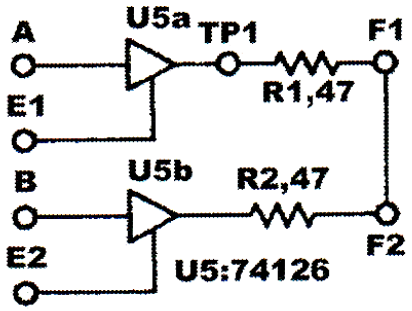


Fig.2-33

2. Connect inputs A to SW0; E1 to SW1; B to SW2; E2 to SW3.Set SW1 and SW3 (E1 and E2) to "1". Follow the input sequences in Table 2-15, measure and record voltages between F1 and TP1.

INPUT E1=E2="1"		OUT	
SW2(B)	SW1(A)	F1=F2	V_{TP1-F1}
0	0		V
0	1		V
1	0		V
1	1		V

Table 2-15

2. Measure the voltage across R1 when E1 > E2 and A /B. Is there any voltage drop across R1?

3. Connect inputs E1~E4 together and insert connection clips according to Fig. 2-34. Change the inputs randomly, observe output at F. Which input determines the output?

4.

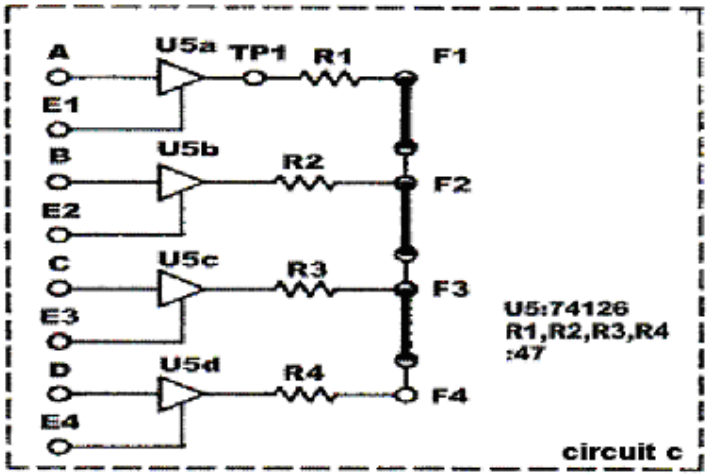


Fig. 2-34 shown the module of DLLT-EM3

When E1="1" and E2=E3=E4="0", F= _____.
When E2="1" and El =E3=E4="0", F= _____.
When E3="1" and E1=E2=E4="0", F= _____.
When E4="1" and El =E2=E3="0", F= _____ .

(c) Bidirectional Transmission Circuit

1. Insert connection clips according to Fig. 2-35 to construct the bidirectional transmission circuit shown in Fig. 2-36.

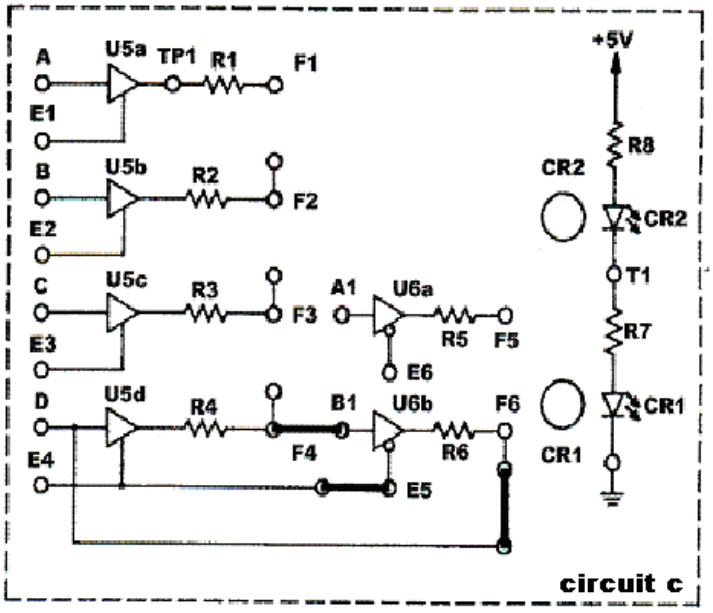


Fig. 2-35

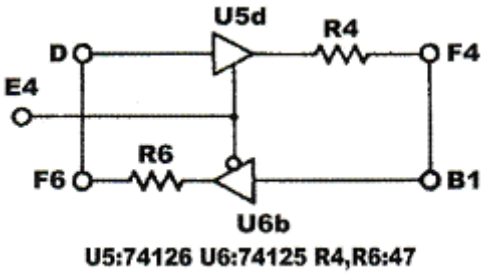


Fig. 2-36

2. Connect F4 and F6 to Logic Indicators L1 and L2. Connect E4 (E4=E5) to SW0. Use SW1 to control the inputs.

   Observe L1 (F4) when SW0="1" and SW1 is connected to D. What is the response of F4 if D goes from "1" to"0" to "1 "?

   Observe L2 (F6) when SW0="0" and SW1 is connected to B. What is the response of F6 if B goes from "1" to "0" to "1 "?

RESULTS

1. Tristate gates are very similar to open-collector gates but only one gate can be activated at a time if tristate gates are connected in parallel.

2. Tristate gates can be triggered by either "0" or "1 ".

3. Unlike the open-collector gate, the tristate gate does not need external resistor or load to operate.

4. Tristate gates are used in complicated circuits such as memory circuits; shift register circuits; multiplexer and demultiplexer circuits. Usually they are connected in parallel and only one gate is triggered at a time.

FAULT SIMULATION

Regardless of the input states, there are no output voltages at the output of U5d. Try to determine possible faults.

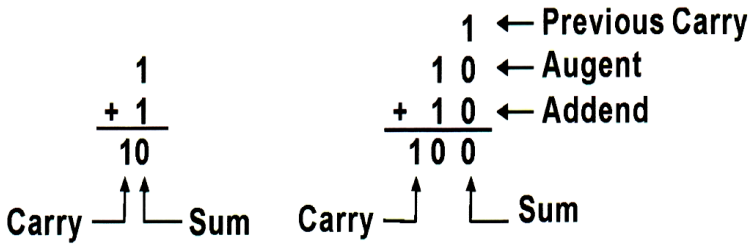
3-2 Half-Adder and Full-Adder Circuit

OBJECTIVE

Understand the characteristics of half-adder and full-adder in the arithmetic unit.

DISCUSSIONS

Adders can be divided into "Half-Adder" (HA) and "Full-Adder" (FA). Half-adders follow the rules of binary addition and consider only the addition of 1 bit. The result of addition is a "carry" and a "sum". In binary additions, a "carry" is generated when the sum of two numbers are greater than 1. Refer to the half-adder addition below:



When "1" and "1" are added the sum is 0 and the carry is 1. The half-adder is limited to the addition of 1-bit numbers.

The full-adder can perform additions of numbers greater than 2-bits in length. Refer to the full-adder operation shown below. It can be constructed using two half-adder. Fig. 2-37 (a) and (b) shows half-adder and full-adder circuits and symbols respectively.

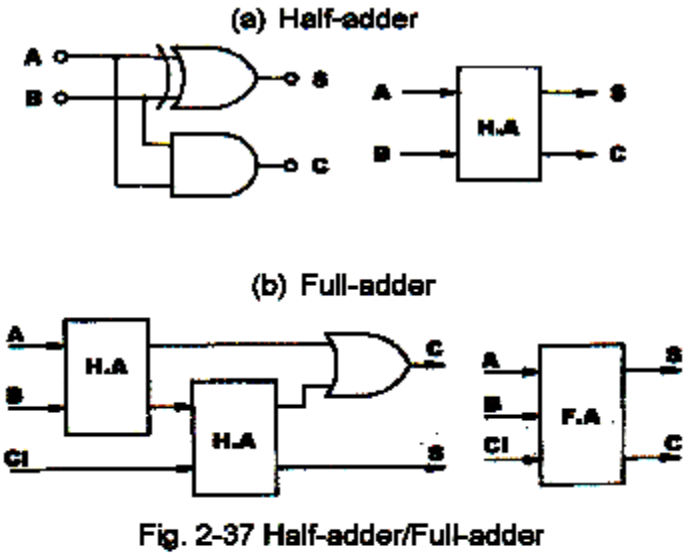


Fig. 2-37 Half-adder/Full-adder

To perform additions of numbers greater than 2-bits in length, the connection shown in Fig. 2-38, or "Parallel Input" should be used to generate sums simultaneously.

However, the sum of the next adder will be stable only after the previous adder's carry has stabilized. For example, in Fig. 2-38, the sum of FA2 will not be stable unless the carry of FA1 is stable.

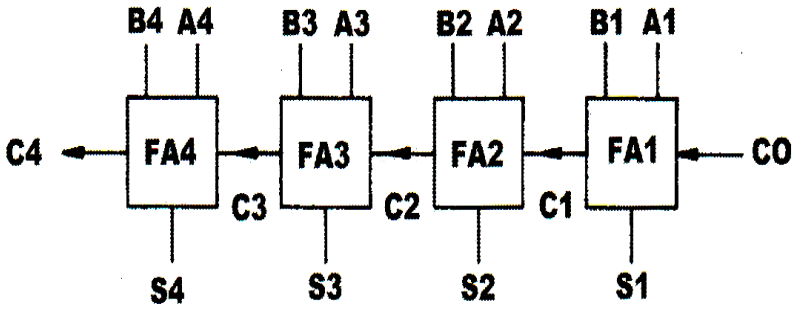


Fig. 2-38

When FA1 adds A1 and B1, a sum S1 and a carry C1 is generated. C1 will be added to A2 and B2 by FA2, generating another sum S2 and another carry C2. In the case of Fig. 2-38, sum of the four adders do not stabilize at the same time, delaying the adding process. This delay can be eliminated by using the "Look-Ahead" adder.

Look-ahead adders do not have to wait for the previous adder to stabilize before performing the next addition, saving valuable time. In Boolean expression we assume'.

$Pi = Ai \oplus Bi$
$Gi = Ai \times Bi$

The output and carry can be expressed as :

$Si = Pi \oplus Ci$

$C_{i+1} = G_i + P_iC_i$

Gi is called "Carry Generate". When Ai and Bi are both "1", Gi is "1" and unrelated to the carry input.

Pi is called "Carry Transmit", related to the carry transmit between Ci and Ci+1.

If we substitute the carry function of each stage by the previous carry we get:

$C_2 = G_1 + P_1C_1$
$C_3 = G_2 + P_2C_2 = G_2+P_2G_1 + P_2P_1C_1$
$C_4 = G_3 + P_3C_3 = G_3+P_3P_2G_1 + P_3P_2P_1C_1$

Fig. 2-39 shows the carry path of a look-ahead adder. The 74182 is a look-ahead adder TTL IC.

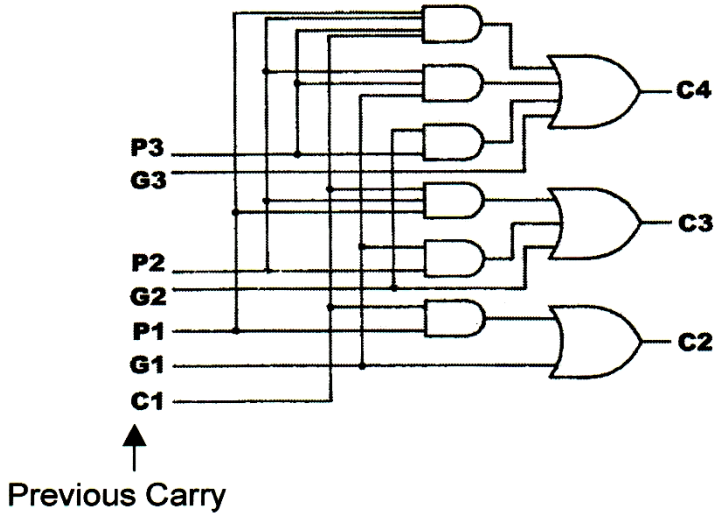


Fig. 2-39

Binary adders can be converted into BCD adders. Since BCD has 4 bits with the largest number being 9; and the largest 4 bit binary number is equivalent to 15, there is a difference of 6 between the binary and the BCD adder. Under the following conditions 6 must be added when binary adders are used to add BCD codes:

1. When there is any carry
2. When the sum is larger than 9

If the order of priority is S8, S4, S2, S1 and the sum is larger than 9 then S8 x S4+S8u x S2. If any carry is involved, assuming the carry is CY, under this term, 6 must be added:

CY+S8xS4+S8xS2

Fig. 2-40 is the circuit of a BCD adder.

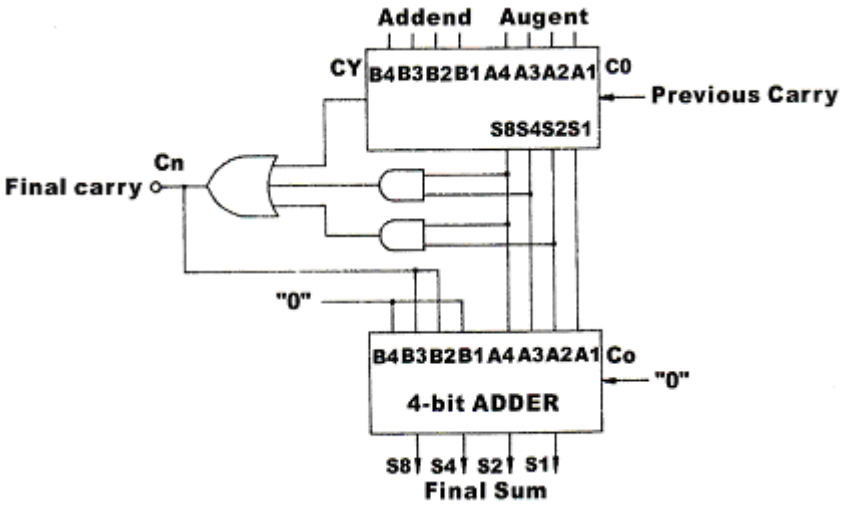


Fig. 2-40

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, Module of DLLT-EM03: Assembled Logic Circuits (2) Experiment

EXERCISE

High- Speed Adder Carry Generator Circuit

1. U3 (74182) on circuit of module DLLT-EM03 is used to construct a carry generator circuit. Fig. 2-45 (b) is the truth table and logic diagram for the 74182.

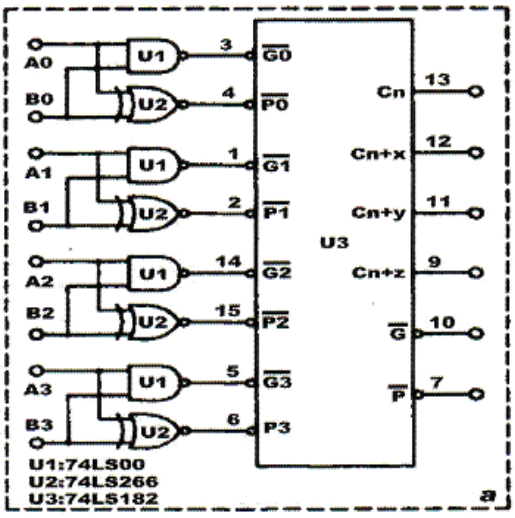


Fig. 2-45 (a)

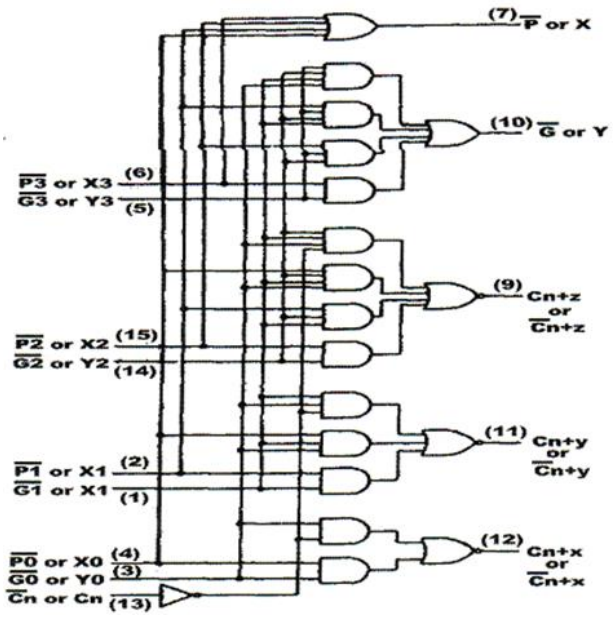

(7) $\overline{P}$ or X
(10) $\overline{G}$ or Y
$\overline{P3}$ or X3 (6)
$\overline{G3}$ or Y3 (5)
(9) Cn+z or $\overline{Cn+z}$
$\overline{P2}$ or X2 (15)
$\overline{G2}$ or Y2 (14)
(11) Cn+y or $\overline{Cn+y}$
$\overline{P1}$ or X1 (2)
$\overline{G1}$ or X1 (1)
(12) Cn+x or $\overline{Cn+x}$
$\overline{P0}$ or X0 (4)
$\overline{G0}$ or Y0 (3)
$\overline{Cn}$ or Cn (13)

Fig. 2-45 (b)

TRUTH TABLE

INPUT									OUTPUTS				
Cn	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	Cn+x	Cn+y	Cn+z	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H=HIGH Voltage Level

L=LOW Voltage Level

X=Immaterial

2. Connect input A0~ A3 (addends) to DIP Switches 1.0 ~ 1.3; Bo~ B3 (augends) to DIP2. ~ 2.3, G and P are triggered by “0”.

$$Cn + x = G0 + P0 \times Cn$$
$$Cn + y = G1 + P1 \times G0 + P1 \times P0 \times Cn$$
$$Cn + z = G2 + P2 \times G1 + P2 \times P1 \times G0 + P2 \times P1 \times P0 \times Cn$$
$$\overline{G} = \overline{G3 + P3 \times G2 + P3 \times P2 \times G1 + P2 \times P1 \times P0 \times G0}$$
$$\overline{P} = \overline{P3 \times P2 \times P1 \times P0}$$

If Cn = 0, then

$$Cn + x = A0 \times B0$$
$$Cn + y = A1 \times B1 + (A0 \oplus B0) \times (A0 \times B0)$$
$$Cn + z = A2 \times B2 + (A2 \oplus B2) \times (A1 \times B1) + (A2 \oplus B2) \times (A1 \oplus B1) \times (A0 \times B0)$$
$$\overline{G} = \overline{A3 \times B3 + (A3 \oplus B3) \times (A2 \times B2) + (A3 \oplus B3) \times (A2 \oplus B2) \times (A1 \times B1) + (A3 \oplus B3) \times (A2 \oplus B2) \times (A1 \oplus B1) \times (A0 \times B0)}$$
$$\overline{P} = \overline{P3 \times P2 \times P1 \times P0}$$

Follow the input sequences in Table 2-19 and record output states.

INPUT								OUTPUT				
B3	B2	B1	B0	A3	A2	A1	A0	Cn+x	Cn+y	Cn+z	$\overline{G}$	$\overline{P}$
0	0	0	1	0	0	0	1					
0	0	1	0	0	0	1	0					
0	0	0	0	0	0	1	0					
0	0	1	1	0	0	1	1					
1	0	1	0	1	0	0	0					
1	1	1	0	1	1	1	1					
1	1	1	1	1	1	0	1					
0	1	1	1	0	1	1	0					
1	0	0	1	0	1	0	1					

Table 2-19

Compare the results with the truth table. Are they identical?
Since Cn= 0, the last carry CY = G.

RESULTS

1. Adders can be further classified into "half-adder" and "full-adder".
2. Binary adders can be converted into BCD code adder.
3. The circuitry of "look-ahead" adder is quite complicated. Unless very high speed is required, it is not used very often.

FAULT SIMULATION

1. Locate the problem(s) if F1 remains at "1" for a full-adder.
2. During BCD code adding operation, F2≠ 1 when F1 =1. What could cause this problem?

3-3 Arithmetic Logic Unit (ALU) Circuit

OBJECTIVE

Understand functions and applications of the ALU, or arithmetic logic unit.

DISCUSSION

In this experiment the 74181 ALU IC will be used to introduce the concept of ALU. Its logic diagram is shown in Fig. 2-54.

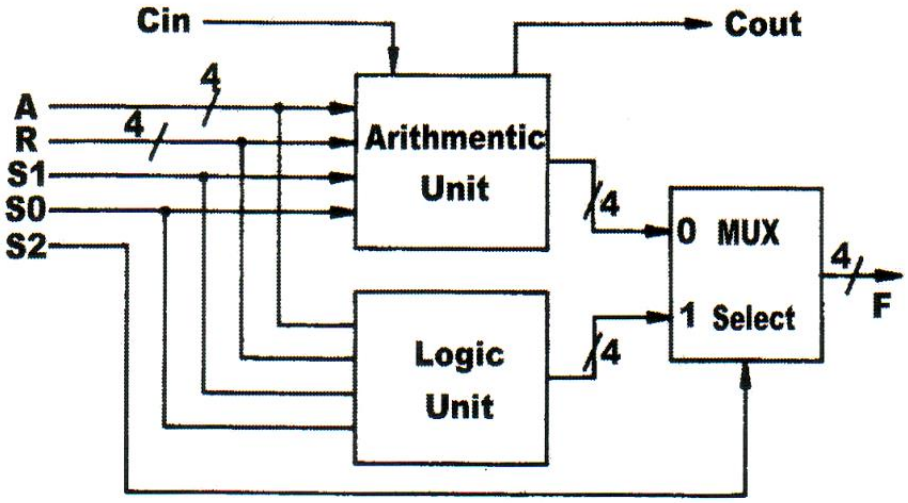


Fig. 2-54

It consists of two major parts: the arithmetic unit and the logic unit. The output, either arithmetic or logic, is selected by a multiplexer (MUX). S2 is the selector gate on the MUX and its state will determine the output of the ALU.

When S2=0, arithmetic operation is executed.

When S2=1, logic operation is executed.

Fig. 2-55 shows the pin assignment and Table 2-33 is the truth table for the 74181.

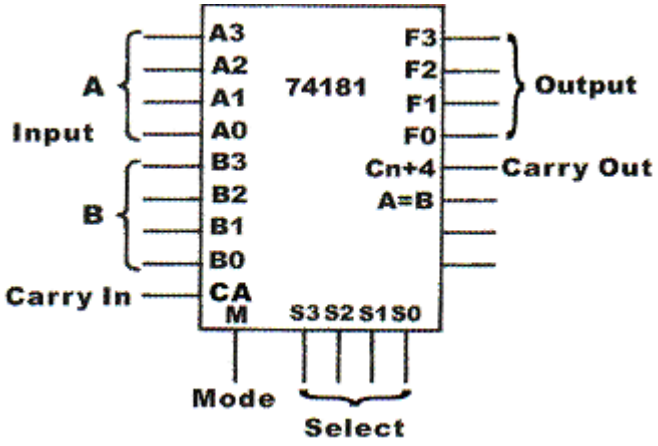


Fig. 2-55

MODE SELECT INPUTS				ACTIVE LOW INPUTS &OUTPUTS		ACTIVE HIGH INPUTS &OUTPUTS	
				LOGIC	ARITHMETIC	LOGIC	ARITHMETIC
S3	S2	S1	S0	(M=H)	(M=L) (C_n=L)	(M=H)	(M=L) (C_n=H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A+B
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{AB}$	$A+\overline{B}$
L	L	H	H	Logical 1	minus 1	Logical 0	Minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	(A+B) plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{AB}$	A plus (A+B)	$\overline{A}+B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A+B)	B	$(A+\overline{B})$ plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logical 0	A plus A	Logical 1	A plus A
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	(A+B) plus A
H	H	H	L	AB	$A\overline{B}$ plus A	A+B	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

Table 2-23

The 74181 has two 4-bit inputs A and B, as well as a "carry-in" (CA) input. The purpose of CA is to provide a reverse carry signal (CA=0 when there is a carry). There is a mode control input (M) and 4 function-select lines S0, S1, S2, S3, forming sixteen logic or arithmetic operations.

The 74181 also has a 4-bit output (F3 ~ F0); a "carry-out" or "Cn+4" output; G (generate) and P (propagate) output. Refer to the truth table of the 74181 in
Table 2-33.

The "+" symbol means OR logic, "Puls" means the sum of inputs. The biggest advantage of the 74181 is its ability to perform arithmetic functions such as addition; subtraction; shifting; and logic functions such as AND; OR and XOR functions.

The mode control input (M) and function-select lines (S0 ~ S3) determines which function it will perform.

The mode control for 74181 is determined by these factors:

1. Addition: A "0" is generated at CA input to signify the existence of a carry. After the arithmetic operation, if the sum is larger than 15, "0" will be generated at CA again.
2. Subtraction: "0" is generates at Cn+4 if the result is "0" or positive. If "0" is generated at CA then the result is negative or there is a borrow. If the result of subtraction is negative, for example "-4", the 4-bit output F will be in 2's complement and Cn+4="1"

EQUIPMENTS REQUIRED
DLLT-1300 Digital Logic Lab Trainer, Module DLLT-EM03: Assembled Logic Circuits (2) Experiment.

EXERCISE

1. Connect function-select lines S3-S0 to Data Switches SW3- SW0 respectively. Connect M to DIP Switch DIP1.6 to select between arithmetic and logic operation. When M="0" arithmetic operation is performed. When M="1" logic function is performed.

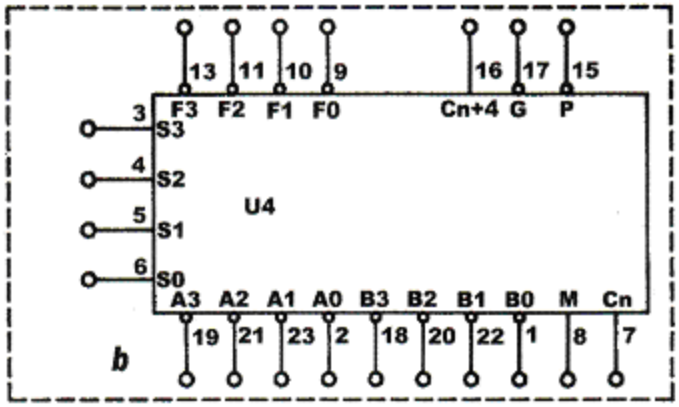


Fig. 2-56

Connect inputs A3 ~ A0 to DIP1.3 ~ 1.0 and B3 ~ B0 to DIP2.3 ~ 2.0; Connect Cn to DIP2.6; outputs F3 ~ F0 to Logic Indicators L4 ~ L1 and Cn+4 to L8. Inputs A3 ~ A0, B3 ~ B0 and outputs F3 ~ F0 are triggered by "0". Low input state is "1" while high input state is "0".

2. Set M to "1" to perform the following logic functions:
   (1) When S3S2S1S0=0000

   What is the output when A3A2A1A0=0000 and B3B2B1 B0=1111?
   What is the output when A3A2A1A0=1100 and B3B2B1 B0=1010?

   (2) When S3S2S1S0=1001

   What is the output when A3A2A1A0=1100 and B3B2B1 B0=0110?
   What is the relationship between the inputs and outputs in terms of logic?

   (3) When S3S2S1S0=1011

   What is the output when A3A2A1A0=0011 and 133132B1 1B0=1001?
   What is the relationship between the inputs and outputs in terms of logic?

3. Set M to "0" to perform the following arithmetic functions:
   (1) Set Cn to "0" and ignore the previous carry

   (A) When S3S2S1S0=1001

   (a) What is the outputs when A3A2A1A0=B3B2B1 B0=0100?

   F3F2F1F0 = _____; Cn+4 = _____

   (b) What is the output when A3A2A1A0=1000 and B3B2B1 B0=1100?

   F3F2F1F0 = _____; Cn+4 = _____

   (B) When S3S2S1 S0=0011

   (a) What is the outputs when A3A2A1A0=0100 and B3B2B1B0=0010?

   F3F2F1F0= _____; Cn+4 = _____

   (b) What is the output when A3A2A1A0=1010 and B3B2B1B0=1000?

   F3F2F1F0= _____; Cn+4 = _____

   (c) When S3S2S1S0=0000

   What is the outputs when A3A2A1A0=1010 and B3B2B1B0=0011?

F3F2F1F0 = _____; Cn+4 = _____

(2) Set Cn to "1", follow the input sequences in Table 2-24 and record the outputs. Depending on the state of M and Cn, function-select line S0 ~ S3 has different functions. Refer to the truth table of 74181 (Table 2-23).

m=0 Cn=1 INPUT															
S3	S2	S1	S0	B3	B2	B1	B0	A3	A2	A1	A0	Cn+4	F3	F2	F1	F0
0	0	0	0	0	0	0	1	0	0	0	1					
0	0	0	0	0	0	1	0	0	0	1	1					
0	0	1	1	0	0	0	1	0	0	1	0					
0	0	1	1	0	1	0	0	0	1	1	0					
0	1	1	0	0	1	0	1	0	1	0	0					
0	1	1	0	0	0	0	1	0	0	1	0					
0	1	1	1	0	1	1	0	0	1	0	1					
0	1	1	1	0	1	1	1	1	0	0	0					
1	0	1	1	1	0	0	0	1	0	0	0					
1	0	1	1	1	1	0	0	0	1	1	0					
1	1	1	1	0	1	1	0	0	1	1	1					
1	1	1	1	0	1	0	1	0	1	1	0					

Table 2-24

RESULTS

The 74181 has 16 arithmetic functions with or without carry, at the same time it is also capable of performing various logic functions. Due to time limitation we did not explore each and every function of the 74181. Such a complicated device is not easy to use unless it is controlled by a computer or a microprocessor.

3-4 Bit Parity Generator Circuit

OBJECTIVE

Understand the construction and applications of bit parity generators.

DISCUSSION

A bit parity, generated by the bit parity generator, usually accompanies the data transmission process. The bit parity provides as a reference point and allows us to compare and check whether the transmission process and the data transmitted are correct or not.

There are two types of bit parity generators: The "Odd" bit parity generator will generate an "1" if the data contains an even number of "1"s. For example the data "10111011" has six "1"s. When the bit parity is added to the end of this data, the number of "1"s in the data will become an "ODD" number, hence the name "Odd Parity Generator".

On the other hand, an "Even" bit parity generator will add an "1" to data with odd number of "1 "s to make the total number of "1"s even. If the data already has an even number of "V's no bit parity is generated. Output Y of the "Even" bit parity generator shown in Fig. 2-57 will be 0 if the inputs ABCDEFGH is equal to 10111011.

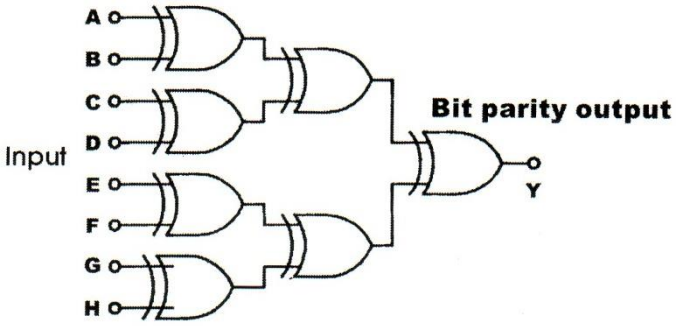


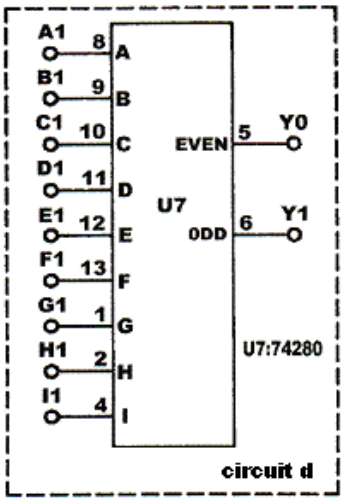
Fig. 2-57 "Even" bit parity generator circuit

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, Module DLLT-EM03: Assembled Logic Circuits (2) Experiment Module

EXERCISE

Bit Parity Generator IC



	OUTPUTS	
	EVEN	ODD
0 2 4 6 8	H	L
1 3 5 7 9	L	H

Fig. 2-60

2. U7 on circuit d of module DLLT-EM03 is a bit parity generator IC. Connect inputs A1, B1, C1, D1, E1, F1, G1, H1 and I1 to DIP Switches 1.0 ~ 1.7 respectively. Connect outputs Y0 to L1; Y1 to L2. Follow the input sequences given in Table 2-26 and record the outputs.

I	H	G	F	E	D	C	B	A	y0 (even)	y1 (odd)
0	0	0	0	0	0	0	0	0		
0	0	0	0	0	0	0	0	1		
0	0	0	0	0	0	0	1	1		
0	0	0	0	0	0	1	1	1		
0	0	0	0	0	1	1	1	1		
0	0	0	0	1	1	1	1	1		
0	0	0	1	1	1	1	1	1		
0	0	1	1	1	1	1	1	1		
0	1	1	1	1	1	1	1	1		
1	1	1	1	1	1	1	1	1		
1	1	1	1	1	1	1	0	1		
1	1	1	1	1	1	1	0	0		
1	1	0	0	0	1	1	0	0		

Table 2-26

RESULTS

1. Bit parity generators can be constructed with XOR gates.

2. There are two types of bit parity: "Odd" and "Even".

FAULT SIMULATION

1. If output F6 of the even bit generator circuit shown in Fig. 2-59 has incorrect output, what could be the problem?

DLLT-EM04 COMBINATIONAL LOGIC CIRCUITS

4-1 Half-Adder and Full-Adder Circuit
- a. Constructing HA with Basic Logic Gates
- b. Full-Adder Circuit with IC
- c. BCD Code Adder Circuit

4-2 Half-Subtractor and Full-Subtractor Circuit
- a. Subtractor Circuit Constructed with Basic Logic Gates
- b. Full-Adder and Inverter Circuit

4-3 Bit Parity Generator Circuit
- a. Bit Parity Generator Constructed with XOR Gates

4-4 Decoder Circuit
- a. Constructing a 4-to-10 Decoder with TTL IC

COMBINATIONAL LOGIC CIRCUITS EXPERIMENTS

Combinational logic circuits are constructed with basic logic gates. Its output will correspond only to the current input, previous inputs and outputs can't influence the current output. Therefore the output of any combinational logic circuits can be expressed by Boolean functions.

The major component of a combinational logic circuit includes Input Variables; Logic Gates and Output Variables. The input variable could be either higher or lower than the output variable but both are binary signals, or "0" and "1".

Assuming there are "n" input variables, there will be 2 possible input combinations, each with one corresponding output combination. Before designing and constructing a combinational logic circuit the following information should be taken into consideration:

1. Truth tables of logic gates
2. Boolean Function
3. Karnaugh Map
4. de Morgan's Theorem

The following combinational logic gates are used very often and they are discussed in this chapter, along with many other combinational logic gates.

1. Combinational logic circuits with NAND and NOR gates
2. AND-OR-INVERTER (A-O-I) gate
3. XOR gate
4. Open-collector gates
5. Tristate gate
6. Arithmetic circuits
7. Encoder and decoder circuits
8. Multiplexer and demultiplexer circuits
9. Comparator circuits

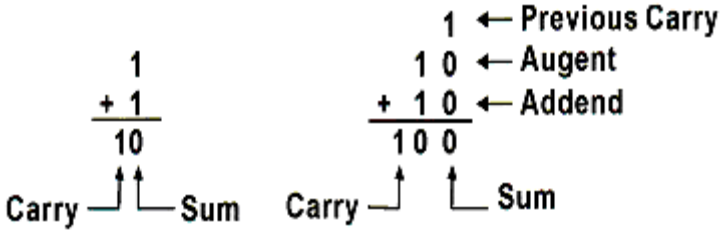
4-1 Half-Adder and Full-Adder Circuit

OBJECTIVE

Understand the characteristics of half-adder and full-adder in the arithmetic unit.

DISCUSSIONS

Adders can be divided into "Half-Adder" (HA) and "Full-Adder" (FA). Half-adders follow the rules of binary addition and consider only the addition of 1 bit. The result of addition is a "carry" and a "sum". In binary additions, a "carry" is generated when the sum of two numbers are greater than 1. Refer to the half-adder addition below:



When "1" and "1" are added the sum is 0 and the carry is 1. The half-adder is limited to the addition of 1-bit numbers.

The full-adder can perform additions of numbers greater than 2-bits in length. Refer to the full-adder operation shown below. It can be constructed using two half-adder. Fig. 2-37 (a) and (b) shows half-adder and full-adder circuits and symbols respectively.

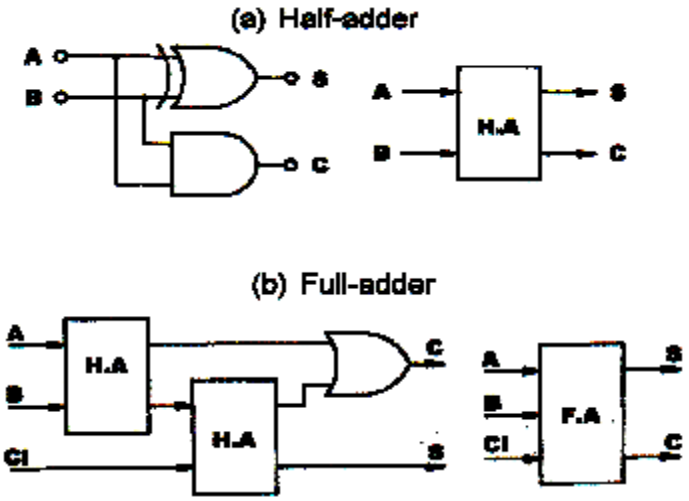


Fig. 2-37 Half-adder/Full-adder

To perform additions of numbers greater than 2-bits in length, the connection shown in Fig. 2-38, or "Parallel Input" should be used to generate sums simultaneously.

However, the sum of the next adder will be stable only after the previous adder's carry has stabilized. For example, in Fig. 2-38, the sum of FA2 will not be stable unless the carry of FA1 is stable.

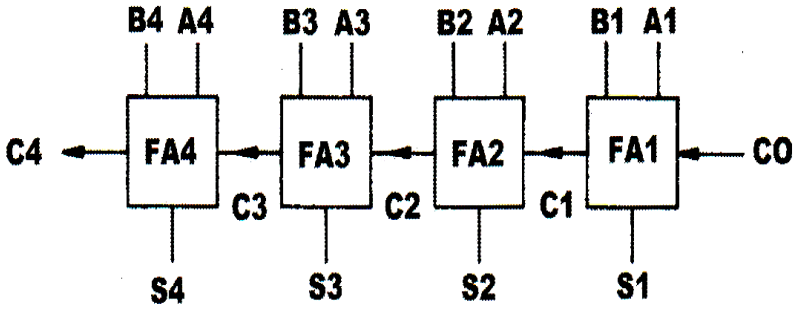


Fig. 2-38

When FA1 adds A1 and B1, a sum S1 and a carry C1 is generated. C1 will be added to A2 and B2 by FA2, generating another sum S2 and another carry C2. In the case of Fig. 2-38, sum of the four adders do not stabilize at the same time, delaying the adding process. This delay can be eliminated by using the "Look-Ahead" adder.

Look-ahead adders do not have to wait for the previous adder to stabilize before performing the next addition, saving valuable time. In Boolean expression we assume'.

$Pi = Ai \oplus Bi$
$Gi = Ai \times Bi$

The output and carry can be expressed as :

$Si = Pi \oplus Ci$
$Ci+1 = Gi + PiCi$

Gi is called "Carry Generate". When Ai and Bi are both "1", Gi is "1" and unrelated to the carry input.

Pi is called "Carry Transmit", related to the carry transmit between Ci and Ci+1.

If we substitute the carry function of each stage by the previous carry we get:

$C2 = G1 + P1C1$
$C3 = G2 + P2C2 = G2+P2G1 + P2P1C1$
$C4 = G3 + P3C3 = G3+P3P2G1 + P3P2P1C1$

Fig. 2-39 shows the carry path of a look-ahead adder. The 74182 is a look-ahead adder TTL IC.

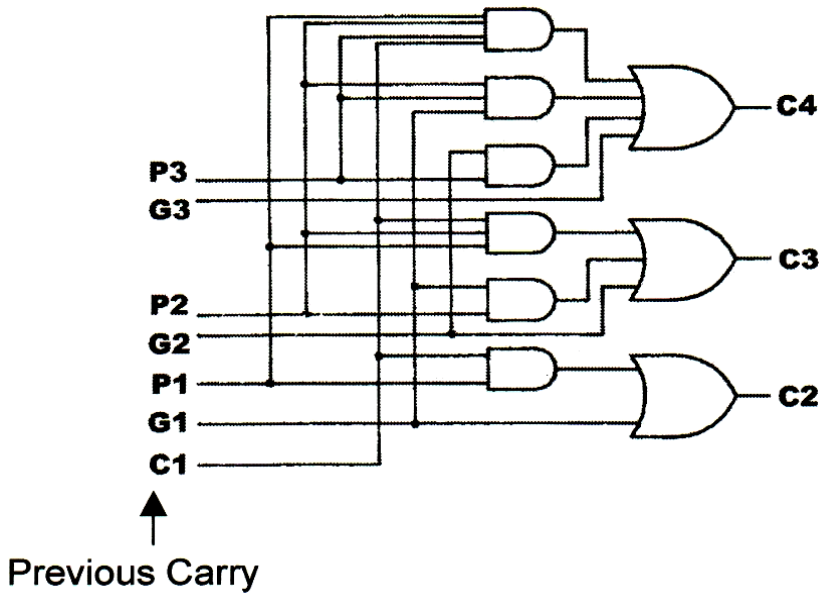


Fig. 2-39

Binary adders can be converted into BCD adders. Since BCD has 4 bits with the largest number being 9; and the largest 4 bit binary number is equivalent to 15, there is a difference of 6 between the binary and the BCD adder. Under the following conditions 6 must be added when binary adders are used to add BCD codes:

1. When there is any carry
2. When the sum is larger than 9

If the order of priority is S8, S4, S2, S1 and the sum is larger than 9 then S8 x S4+S8u x S2. If any carry is involved, assuming the carry is CY, under this term, 6 must be added:

CY+S8xS4+S8xS2

Fig. 2-40 is the circuit of a BCD adder.

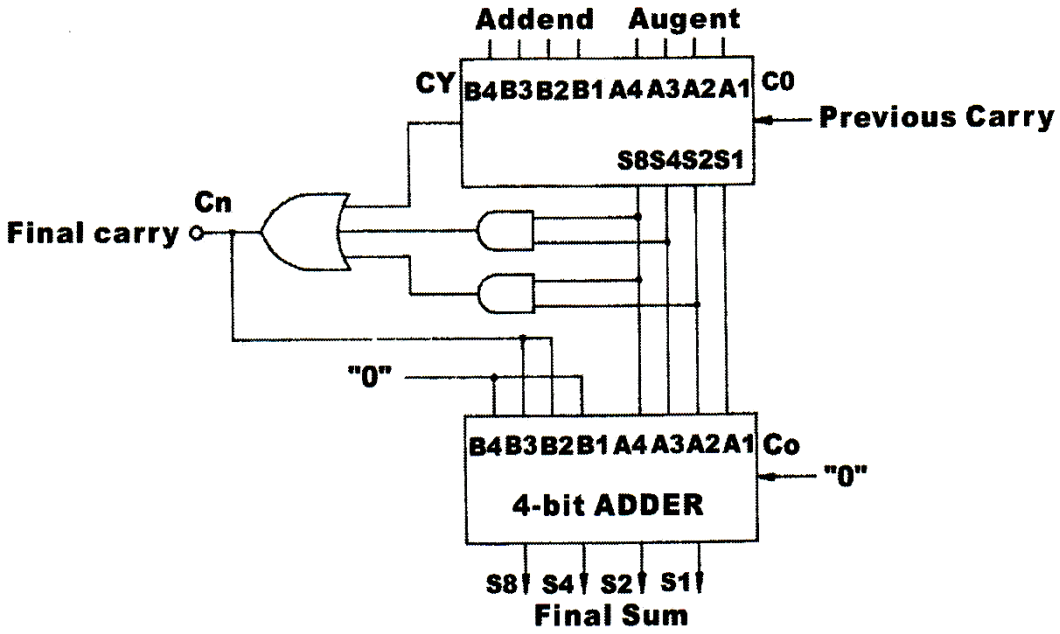


Fig. 2-40

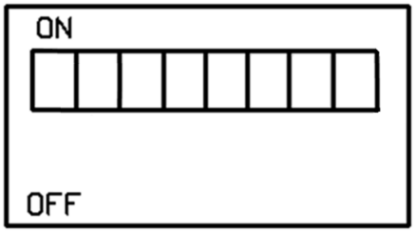
EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, Module of DLLT-EM04: Assembled Logic Circuits (3) Experiment

EXERCISE

(a) Constructing HA with Basic Logic Gates

1. Make sure the Fault Simulator DIP Switch follows the below setting:



2. Insert connection clips according to Fig. 2-41, using U2a and U3a to assemble the half-adder circuit of Fig. 2-42. Connect Vcc to +5V.

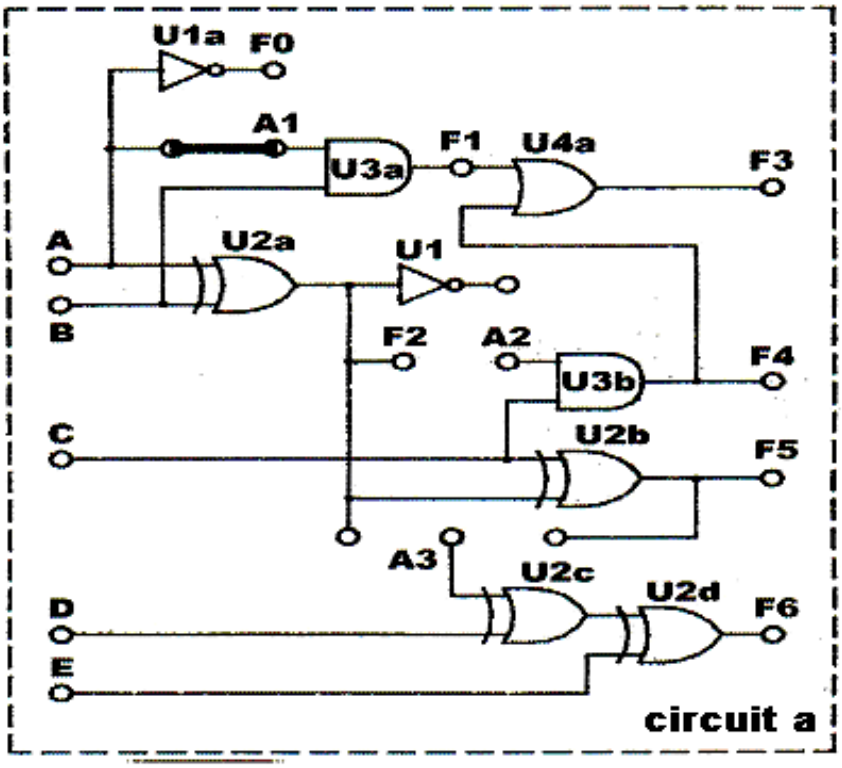


Fig. 2-41

2. Connect inputs A and B to Data Switches SW0 and SW1.Connect outputs F1 and F2 to Logic Indicator L1 and L2. Follow the input sequences for A and B in Table 2-16 and record the output states. Determine which output is the sum and which is the carry

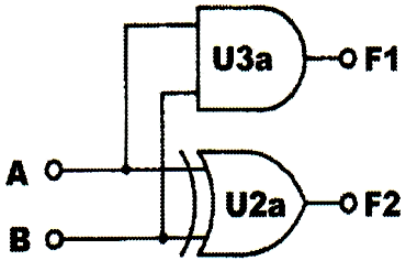


Fig. 2-42

INPUT		OUT	
SW1(B)	SW0(A)	F1	F2
0	0		
0	1		
1	0		
1	1		

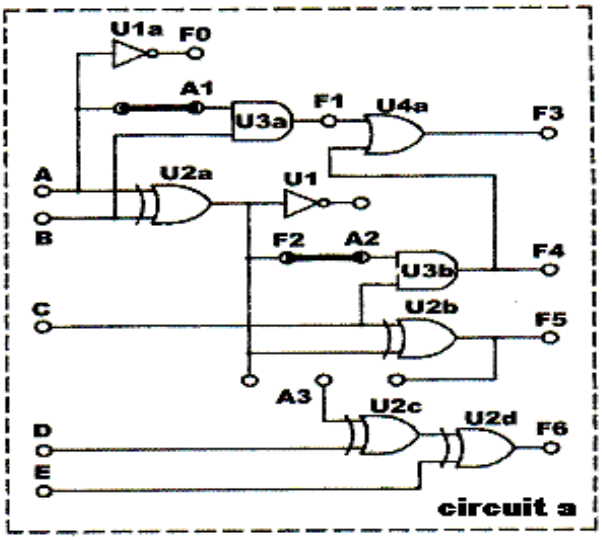
Table 2-16

3. Reassemble the circuit according to Fig. 2-42 (a) to construct the full-adder circuit shown in Fig. 2-42 (b).

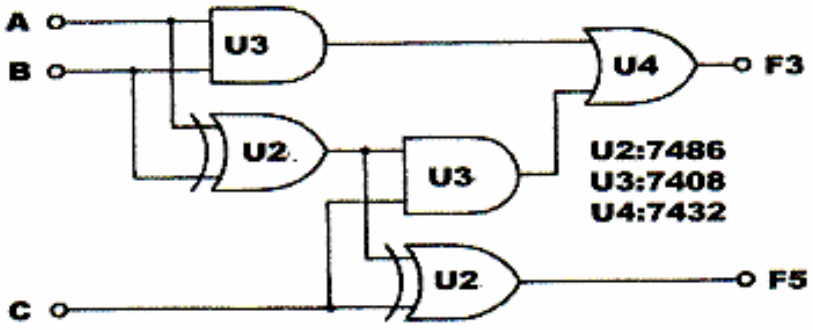
   Connect A, B, C to SW1, SW2 and SW3. A and B are augends while C is the previous carry. Connect F3 to L1, F5 to L2. Follow the input sequences in Table 2-17 and record output states. Determine which output is the sum and which is the carry.

OUTPUT			OUT	
SW3(C)	SW2(B)	SW1(A)	F3	F5
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Table 2-17



(a)



(b)

Fig. 2-43 Full-adder circuit

(b) Full-Adder Circuit with IC

1. U5 on circuit b of module DLLT-EM04 is used as a 4-bit adder. Connect input Y5 to "0", so the XOR gates U6a-U6d, which are connected to Y0 ~Y3, will act as buffers. Connect inputs X0 ~ X3 (addends), Y0 ~ Y3 (augends) to DIP Switches DIP2.0 ~ 2.3 and DIP1.0 ~ 1.3 respectively. Connect F1, Σ0, Σ 1, Σ 2, Σ 3 to L1 ~ L5. Follow input sequences in Table 2-18, record F1 and Σ in hexadecimal numbers.

(X and Y can also be connected to the Thumbwheel Switches)

X=X3X2X1 X0
Y=Y3Y2Y1 Y0
Σ= Σ 3 Σ2 Σ1 Σ0

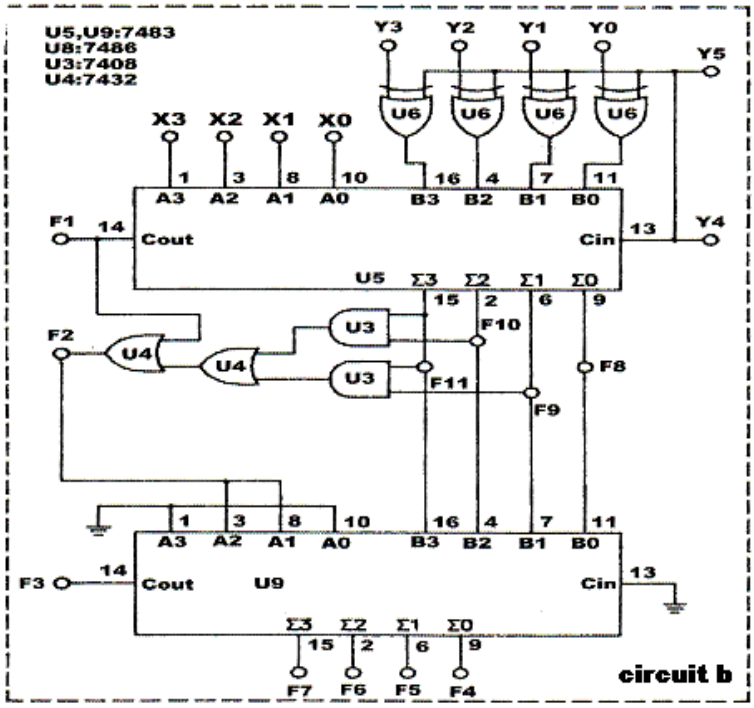


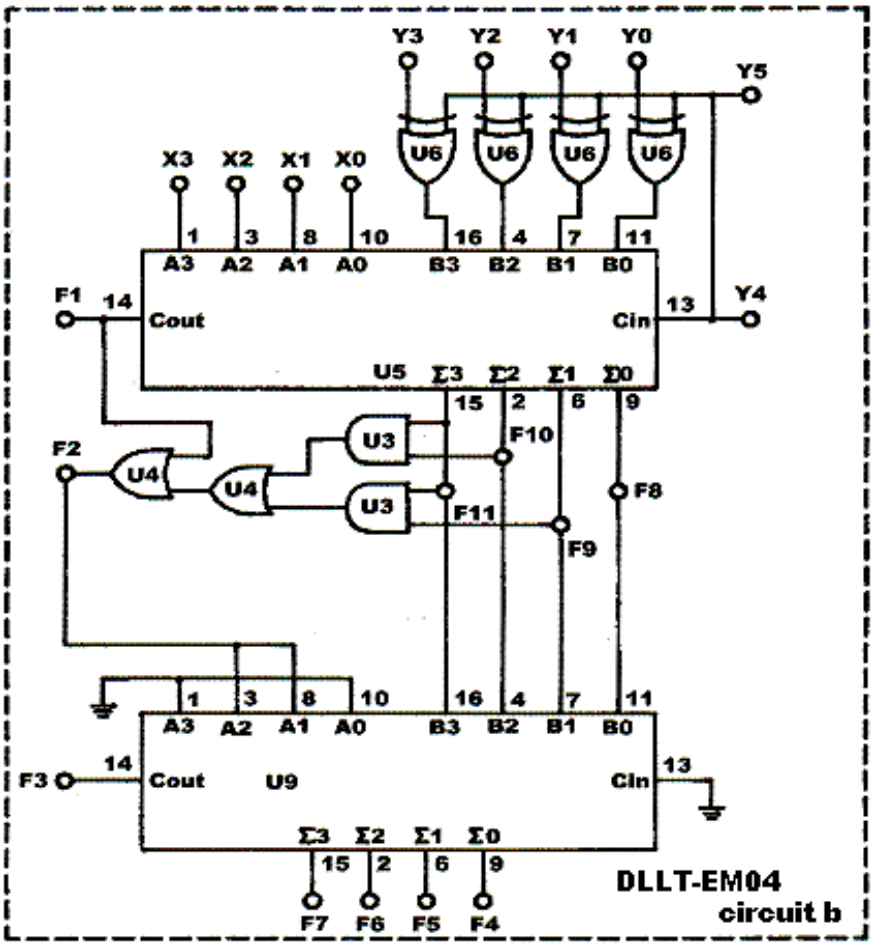
Fig. 2-44

INPUT		OUTPUT	
Y	X	Σ	F1(CARRY)
0	0		
0	1		
0	6		
0	9		
0	F		
1	3		
1	6		
1	8		
3	6		
4	8		
4	F		
8	7		
9	9		
A	B		
C	E		
F	F		

Table 2-8

(c) BCD Code Adder Circuit

1. The circuit shown in Fig. 2-46 will act as a BCD code adder.



2. Connect input X0~ X3 to DIP1.0 ~ 1.3; Y0~ Y3 to DIP2.0 ~ 2.3: Y5 to “0”. Fig. 2-47 is the equivalent circuit.

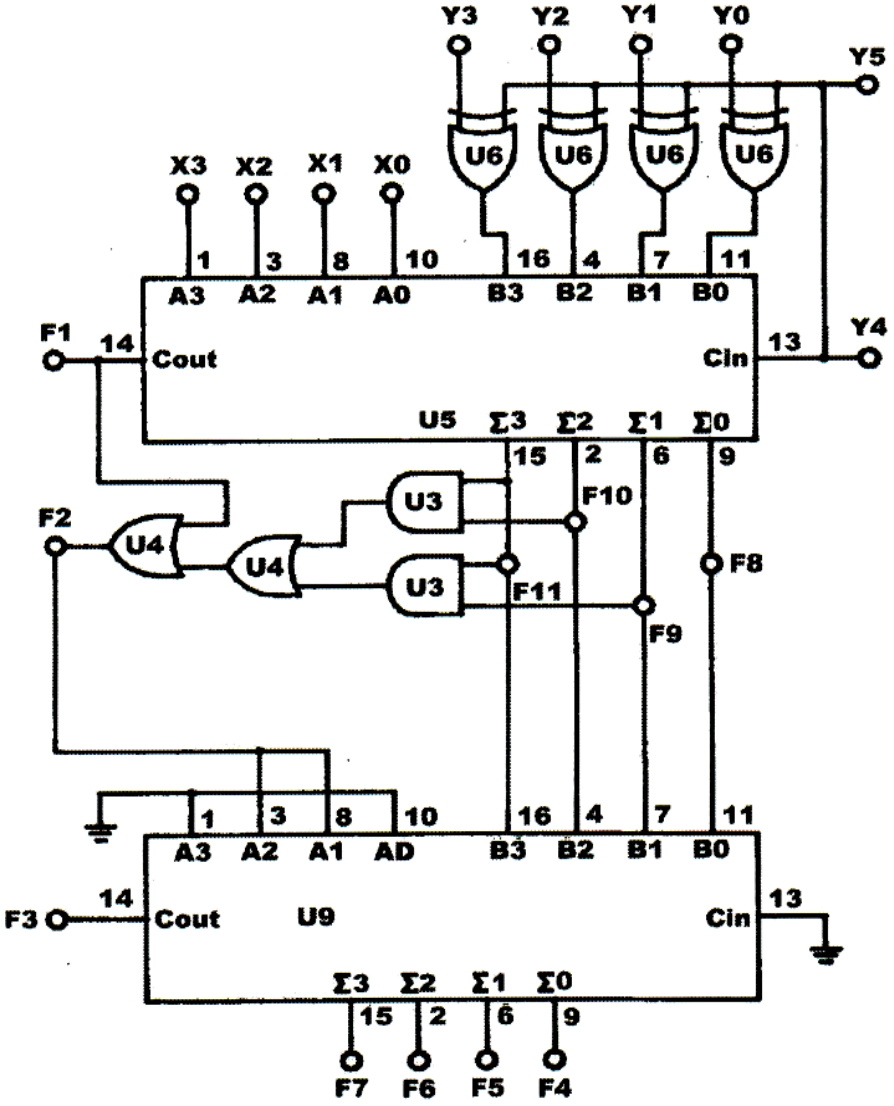


Fig 2-47

U5 and U9 are 7483 look-ahead 4-bit BCD adders, connect outputs F8 ~ F11 of U5 the inputs of one of the 7-Segment Digital Display. F8 ~ F11 should also be connected to L1 ~ L4. Connect F1, F2 to Logic Indicators L5, and L6.

Connect outputs F4 ~ F7 of U9 to another 7-segment display. Also connect F4 ~ F7 to L7 ~ L10 and F3 to L11.

3. F11-F8 are the sum of X0 ~ X3 added to Y0 ~ Y3 while F1 is the carry. Follow the input sequences for X0 ~ X3 and Y0 ~ Y3 in Table 2-20 and record the output states.

INPUT								OUTPUT(U5)					LAST(U9)					
X3	X2	X1	X0	Y3	Y2	Y1	Y0	F1	F11	F10	F9	F8	F2	F3	F7	F6	F5	F4
0	0	0	0	0	0	0	0											
0	0	0	1	0	0	1	1											
0	0	1	1	0	1	0	0											
0	0	1	0	0	0	1	0											
0	0	1	0	1	0	0	0											
0	0	1	1	0	1	1	0											
0	1	0	0	0	0	1	0											
0	1	0	0	0	1	0	1											
0	1	0	0	0	1	1	0											
0	1	0	1	0	1	1	0											
0	1	1	0	0	1	1	1											
0	1	1	1	1	0	0	0											
0	1	1	1	1	0	0	1											
1	0	0	0	1	0	0	1											
1	0	0	1	1	0	0	1											
1	0	1	0	1	0	1	0											
1	0	1	0	1	0	1	1											
1	0	1	0	1	1	0	0											
1	0	1	1	1	1	1	0											
1	1	1	1	1	1	1	1											

Table 2-20

4. Connect inputs X0 ~ X3, Y0 ~ Y3 to the Thumbwheel Switches and outputs F7 ~ F4 to the 7-segment digital display. Adjust the inputs randomly and observe the outputs.

RESULTS

4. Adders can be further classified into "half-adder" and "full-adder".
5. Binary adders can be converted into BCD code adder.
6. The circuitry of "look-ahead" adder is quite complicated. Unless very high speed is required, it is not used very often.

FAULT SIMULATION

1. Locate the problem(s) if F1 remains at "1" for a full-adder.
2. During BCD code adding operation, F2≠ 1 when F1 =1. What could cause this problem?

4-2 Half-Subtractor and Full-Subtractor Circuit

OBJECTIVE

Understand the theory of complements and construction of subtractor circuits.

DISCUSSION

Half-subtractor and full-subtractor circuits can be built by referring to the truth tables and the Boolean expressions, or Karnaugh's map of logic gates. In this experiment we will use the theory of complement to assemble full and half subtractor circuits.

Binary subtractions are usually performed by 2's complement. Two steps are required to obtain 2's complement. First, the subtrahend is inverted to its 1's complement, i.e. an "1" to a "0" and a "0" to an "1". Secondly, an "1" is added to the least significant digit of the subtrahend in 1's complement.

In general subtraction the subtrahend is directly subtracted from the minuend but in 2's complement, the two numbers are added. Hence an adder also can be used as a subtractor.

EXAMPLE:

What is the equivalent in 2's complement for the decimal subtraction of 11 - 10?

MINUEND : 11 (DECIMAL) = 1011 (BINARY)

SUBTRAHEND : 10 (DECIMAL) = 1010 (BINARY)
= 0101 (1'S COMPLEMENT)
= 0110 (2'S COMPLEMENT)

DECIMAL	BINARY	1'S COMPLEMENT	2'S COMPLEMENT
11	1011	1011	1011
− 10	− 1010	− 1011	+ 0110
1	1	0	10001

A carry of “1” is generated in the 2’s complement subtraction.

A half-subtractor execute its task of subtraction 1-bit at a time regardless of whether the minuend is greater or less than the subtrahend. The true table and logic diagram of a half-sub tractor is shown in Fig. 2-48. "Borrow" from previous subtraction are not taken into consideration.

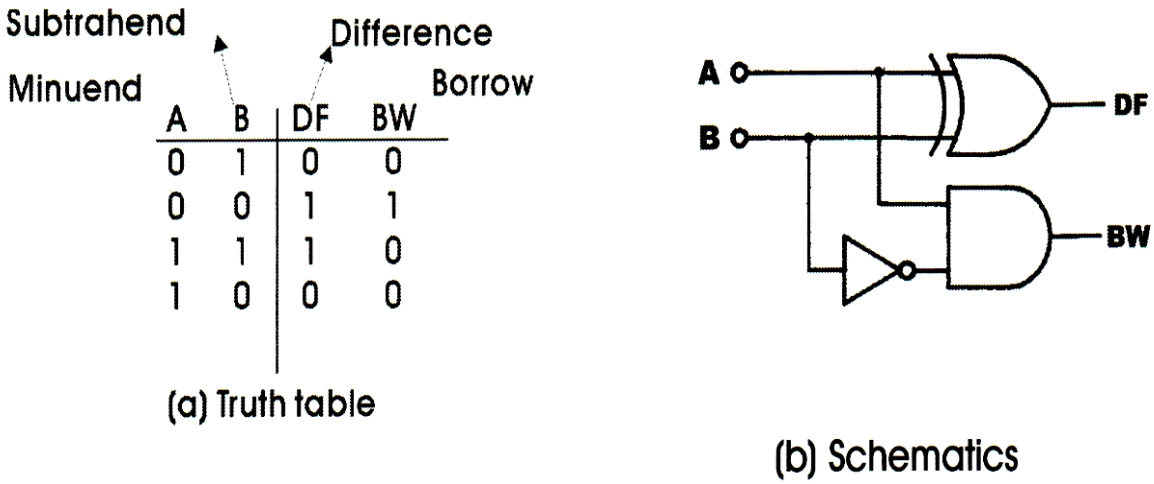


Fig. 2-48 Half- subtractor

Compare the logic diagrams of half-subtractor with half-adder and we can see that the only difference is the inverter at the input of the half-subtractor. This inverter gate represent the borrow.

The full-subtractor has to consider borrow(s) from previous stages. Its truth table and logic diagram are shown in Figure 2-49. When C = "0" it is equivalent to a half-subtractor.
Previous borrow Minuend Subtrahend Difference Borrow

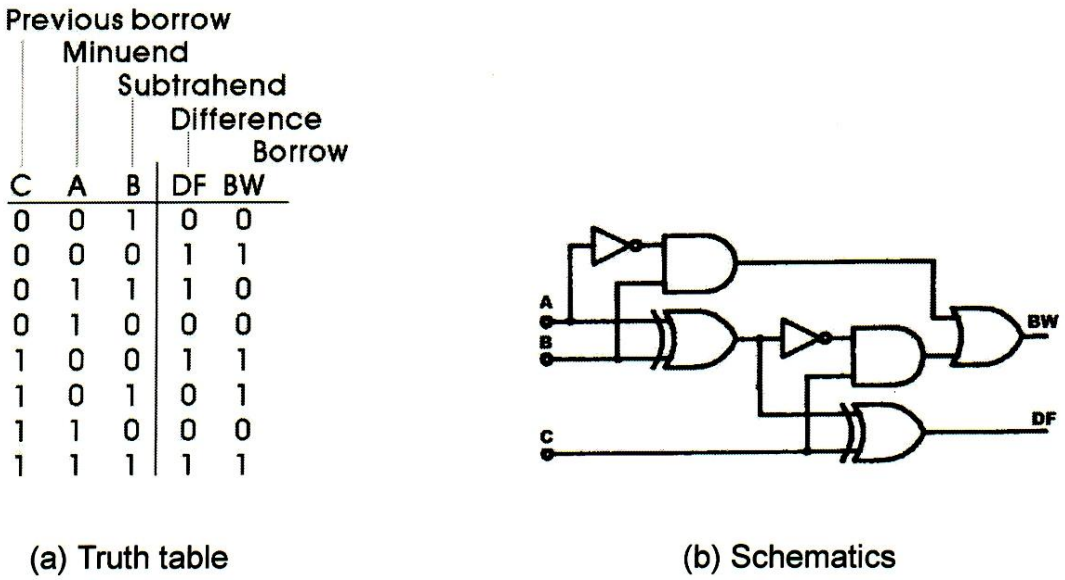


Fig. 2-49 Full-subtractor

From a 4-bit adder circuit we can assemble subtractor circuits of 4-bit or longer. Fig. 2-50 shows a dual-purpose adder/ subtractor circuit. When Bn-1="0" additions are performed and all XOR gates act as buffers. When Bn-1="1" subtractions will be performed and all XOR gates act as NOT gates. Y inputs uses 1's

complement and adds an "1" from Cin. The outputs are Cn (carry) and Bn (borrow), Cn and Bn are dependent on Bn-1.

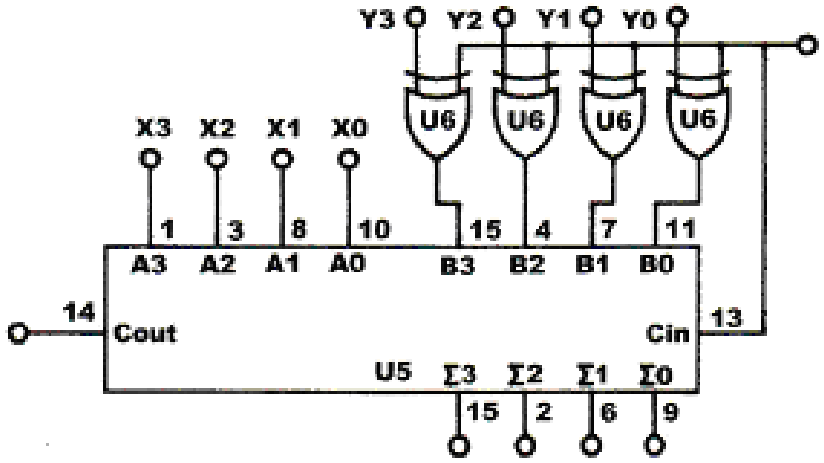


Fig. 2-50

EQUIPMENTS REQUIRED
DLLT-1300 Digital Logic Lab Trainer, DLLT-EM04: Assembled Logic Circuits (3) Experiment Module

EXERCISE

(a) Subtractor Circuit Constructed with Basic Logic Gates

1. Insert connection clips according to Fig. 2-51.

2. Connect inputs A ~ C to Data Switches SW0 ~ SW2; outputs F2 to Logic Indicator L1; F1 to L2; F3 to L3; F5 to L4. When C=0 the circuit is a half-subtractor. F1 is the borrow output; F2 is the difference and F5=F2; F4=0; F3=F1. When C=1 the circuit is a full-subtractor. F3 is the borrow output and F5 is the difference output.

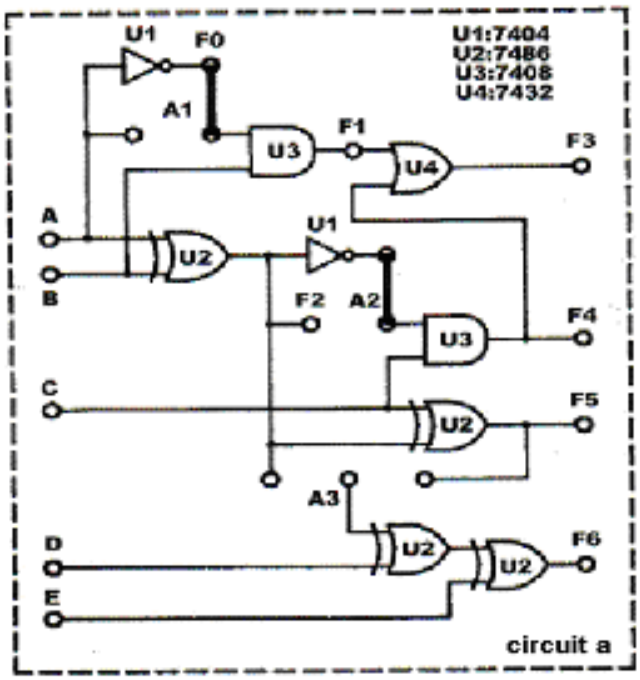


Fig. 2-51 Half-adder/Full-adder

3. Follow the input sequences in Table 2-21 and record output states.

	Input			Difference			
				Borrow		Sum	
	C	A	B	F1	F2	F3	F5
Half-subtractor Half-adder	0	0	1				
	0	0	0				
	0	1	1				
	0	1	0				
Full-subtractor Full-adder	1	0	0				
	1	0	1				
	1	1	0				
	1	1	1				

Table 2-21

(b) Full-Adder and Inverter Circuit

1. The circuit of Module DLLT-EM04 circuit b (Fig. 2-52) is equivalent to the adder/subtractor circuit of Fig. 2-53.

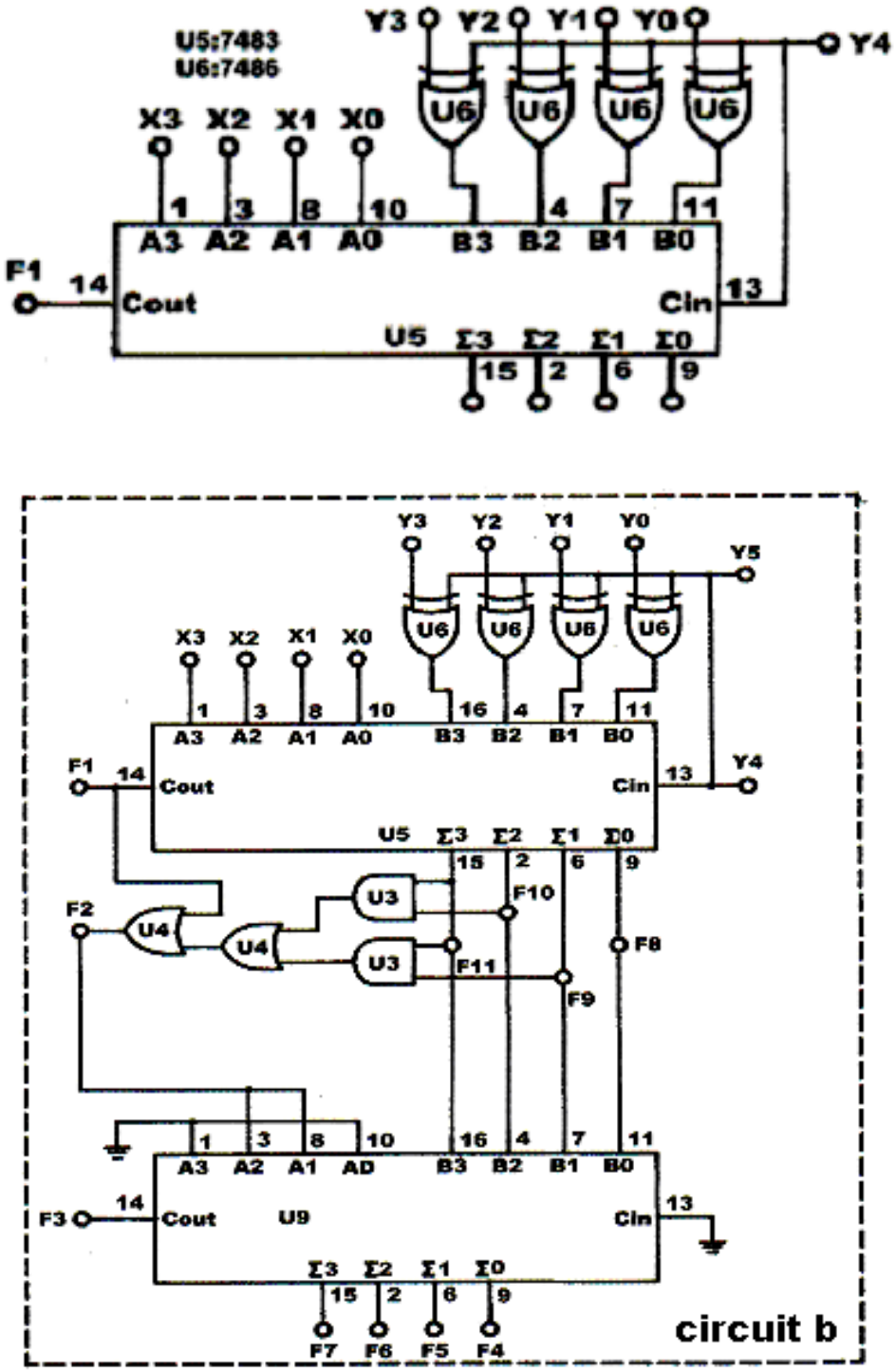


Fig. 2-53 Adder/subtractor

2. Connect inputs X3 ~ X0 to DIP Switch 1.3 ~ 1.0; Y3 ~ Y0 to DIP 2.3 ~ DIP2.0; Y5 to SW0. Connect outputs F1 to L1; F11 ~ F8 to L5 ~ L2. To execute the subtract operation, connect Y5 to "1" (or Cin of U5=1). Follow the input sequences below and record the output states in Table 2-22.

INPUT								OUTPUT				
X3	X2	X1	X0	Y3	Y2	Y1	Y0	F1	F11	F10	F9	F8
0	1	0	0	0	1	0	0					
0	1	0	0	0	0	1	1					
1	0	0	0	0	0	1	1					
1	0	0	0	0	0	0	1					
1	0	0	1	1	0	0	0					
1	0	0	1	0	1	1	1					
1	0	1	0	0	1	1	0					
1	0	1	0	0	1	0	1					
1	0	1	1	1	0	1	0					
1	1	1	1	1	0	1	0					

Table 2-22

RESULTS

1. A half-subtractor is a half-adder with reversed minuend input.
2. A full-subtractor is a full-adder with reversed minuend input.
3. IC adder uses the "2's complement" method.

FAULT SIMULATION

When Y5="1", the circuit of Fig. 2-52 is supposed to execute the subtraction operation. When Y5="1" the addition operation is supposed to be executed. If Y5="0" and an extra "1" is generated, what could be the problem(s)?

4-3 Bit Parity Generator Circuit

OBJECTIVE

Understand the construction and applications of bit parity generators.

DISCUSSION

A bit parity, generated by the bit parity generator, usually accompanies the data transmission process. The bit parity provides as a reference point and allows us to compare and check whether the transmission process and the data transmitted are correct or not.

There are two types of bit parity generators: The "Odd" bit parity generator will generate an "1" if the data contains an even number of "1"s. For example the data "10111011" has six "1"s. When the bit parity is added to the end of this data, the number of "1"s in the data will become an "ODD" number, hence the name "Odd Parity Generator".

On the other hand, an "Even" bit parity generator will add an "1" to data with odd number of "1 "s to make the total number of "1"s even. If the data already has an even number of "V's no bit parity is generated. Output Y of the "Even" bit parity generator shown in Fig. 2-57 will be 0 if the inputs ABCDEFGH is equal to 10111011.

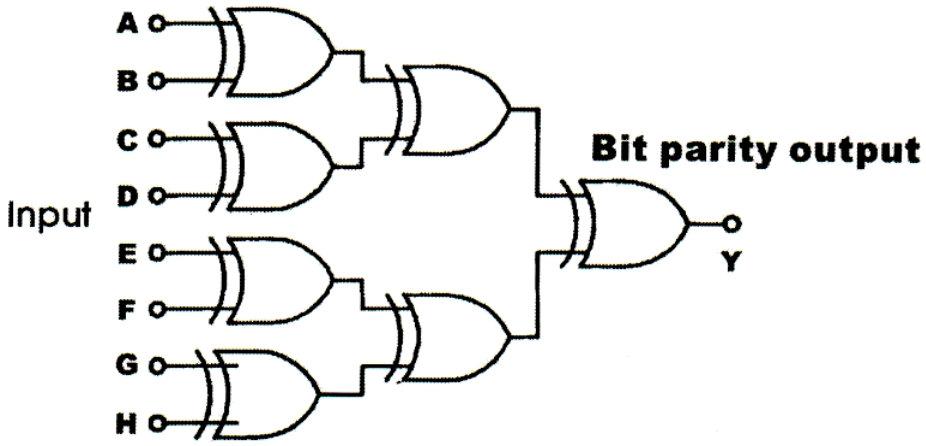


Fig. 2-57 "Even" bit parity generator circuit

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, Module DLLT-EM04: Assembled Logic Circuits (3) Experiment Module

EXERCISE

Bit Parity Generator Constructed With XOR Gates

3. Insert connection clip according to Fig. 2-58 to construct the even bit parity generator circuit of Fig. 2-59.

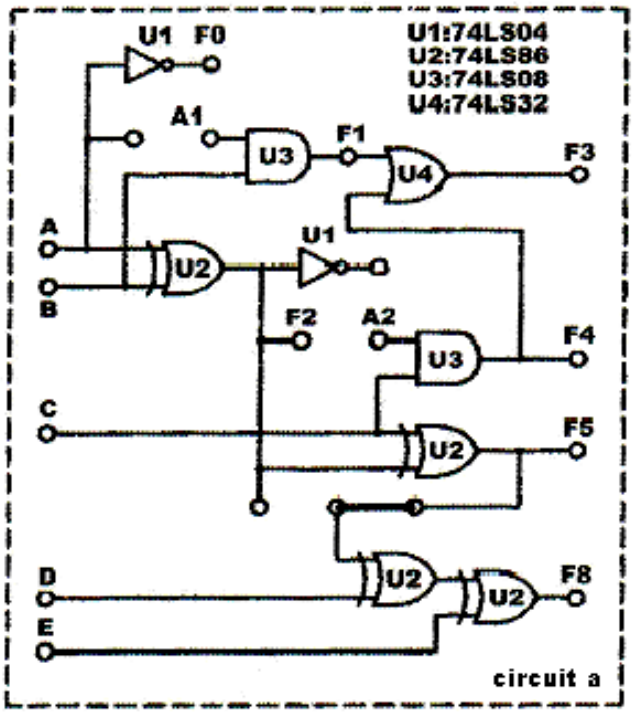


Fig. 2-58

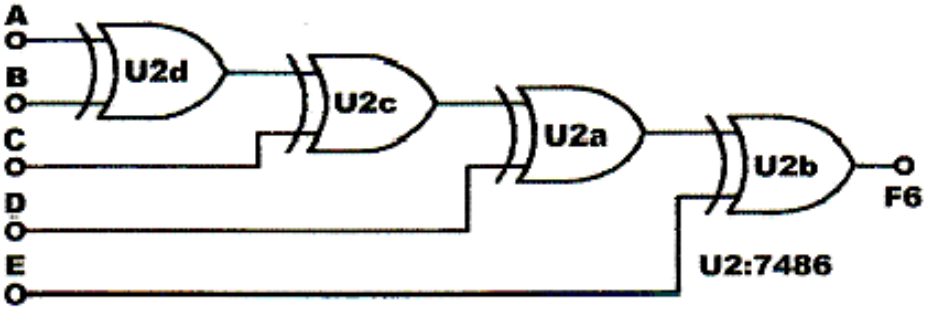


Fig. 2-59 "Even" bit parity generator circuit

3. Connect inputs A, B, C, D, E to DIP Switches 1.0-1.4 and output F6 to Logic Indicator L1. Follow the input sequences in Table 2-25 and record the outputs.

Input					
E	D	C	B	A	F6
0	0	0	0	0	
0	0	0	1	0	
0	0	0	1	1	
0	0	1	0	0	
0	0	1	0	1	
0	1	1	1	0	
1	1	0	0	0	
1	1	0	1	0	
1	1	1	1	0	
1	1	1	1	1	

Table 2-25

RESULTS

3. Bit parity generators can be constructed with XOR gates.

4. There are two types of bit parity: "Odd" and "Even".

FAULT SIMULATION

2. If output F6 of the even bit generator circuit shown in Fig. 2-59 has incorrect output, what could be the problem?

EXERCISE

1. Construct a circuit that transmits 4-bit data with bit parity and see if the outputs are correct.

4-4 Decoder Circuit

OBJECTIVE

Understand the operating principles of decoder circuits.

DISCUSSION

A decoder is a logic circuit that will detect the presence of a specific binary number or word. The input to the decoder is a parallel binary number and the output is a binary signal that indicates the presence or absence of that specific number.

The AND gate can be used as a basic decoder circuit, since the AND gates's output will be a binary 1 only when all inputs are binary 1. Proper connections of AND gate's inputs to the data will ensure detection of any binary number.

Binary-to-Octal Decoder

A binary-to-octal decoder is shown in Fig. 2-67. There are 3 binary inputs A, B, C and 8 octal outputs Q0~Q7. If CBA= "010" output Q2= "1". When CBA= "111" output Q7= "1".

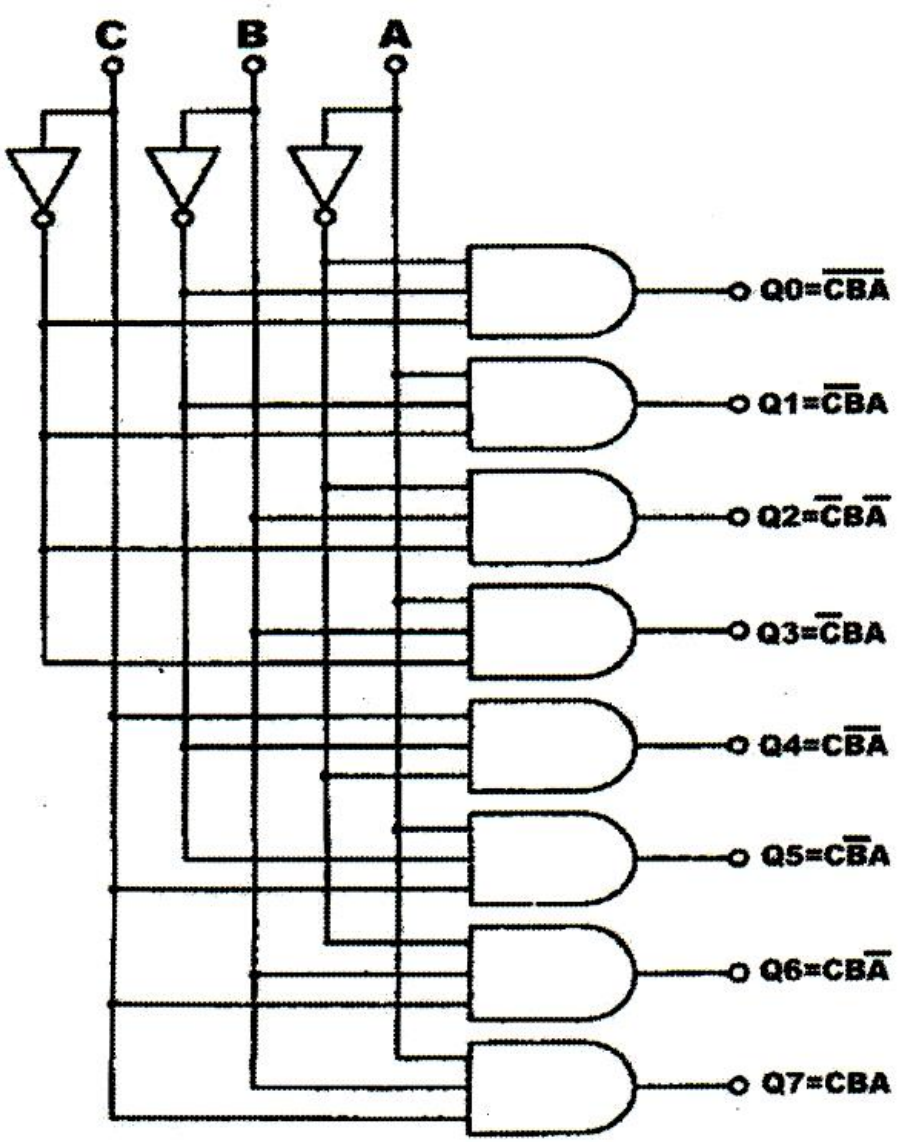


Fig. 2-67

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; Module DLLT-EM04: Assembled Logic Circuits (3) Experiment; Multimeter

EXERCISE

Constructing a 4 to 10 Decoder with TTL IC

1. U10 (7442) on block c of module DLLT-EM04 will be used in this section of the experiment. 7442 is a BCD-to-Decimal decoder IC.

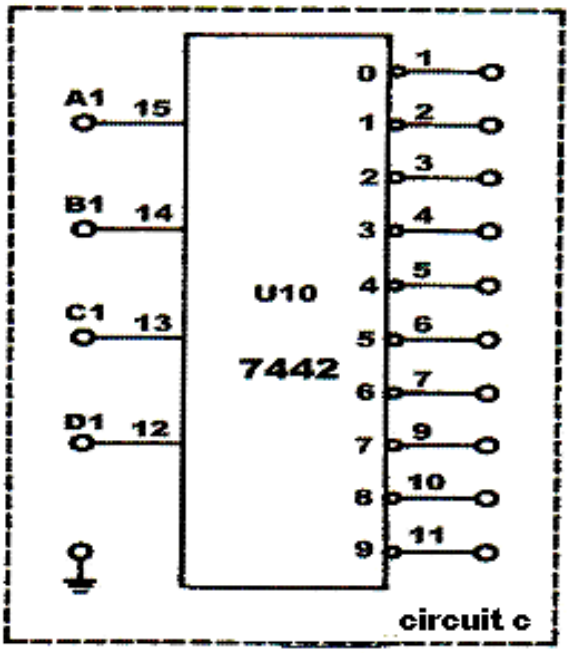


Fig.2-69

3. Connect inputs A1, B1, C1, D1 to the BCD outputs "1", "2", "4", "8" of one of the Thumbwheel Switches respectively. Connect outputs 0-9 to Logic Indicator L0 ~ L9. The thumbwheel switch is a mechanical device that converts numbers to BCD codes.

4. Connect the common to a data switch and switch it to “1”.

5. Adjust the Thumbwheel Switches according to Table 2-32, measure voltages at A, B, C, D with a multimeter. Presence of voltage at the inputs indicates high logic state or "'I", absence of voltage indicates low logic state or "0". Observe the output states at L0 ~ L9. Record input and output logic states in Table 2-32.

	D C B A	0 1 2 3 4 5 6 7 8 9
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		

Table 2-32

RESULTS

1. Decoder has the exact opposite functions of the encoder.

2. Two of the most direct applications of decoders are with numbers and words.

3. The 7442 is a 3 line-to-8 line decoder if D=0.

FAULT SIMULATIONS

1. Two separate input/output sequences for the decoder circuit of Fig. 2-68 are given below. Determine the fault(s) in each case.

B	A	F4	F3	F2	F1
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	0	0	0	0

B	A	F4	F3	F2	F1
0	0	0	1	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

1. Determine the fault(s) if U8 is used as decoder and the outputs are incorrect.

2. The outputs of BCD-to-7-segment decoder are incorrect. Try to determine possible causes.

DLLT-EM05 COMBINATIONAL LOGIC CIRCUITS

5-1 Encoder Circuit
- a. Constructing a 4-to-2 Encoder with Basic Gates

5-2 Decoder Circuit
- a. Constructing a 2-to-4 Decoder with Basic Gates
- b. BCD-to-7-Segment Decoder

5-1 Encoder Circuit

OBJECTIVE

Understand the operating principles of encoder circuits.

DISCUSSION

An encoder is a combinational logic gates that accept one or multiple inputs and generates a specific output code. Only one input is triggered at a time. An encoder with n-bit inputs and n-bit outputs is shown in Fig. 2-61. When one of the inputs is triggered there will be a n-bit output code at the outputs.

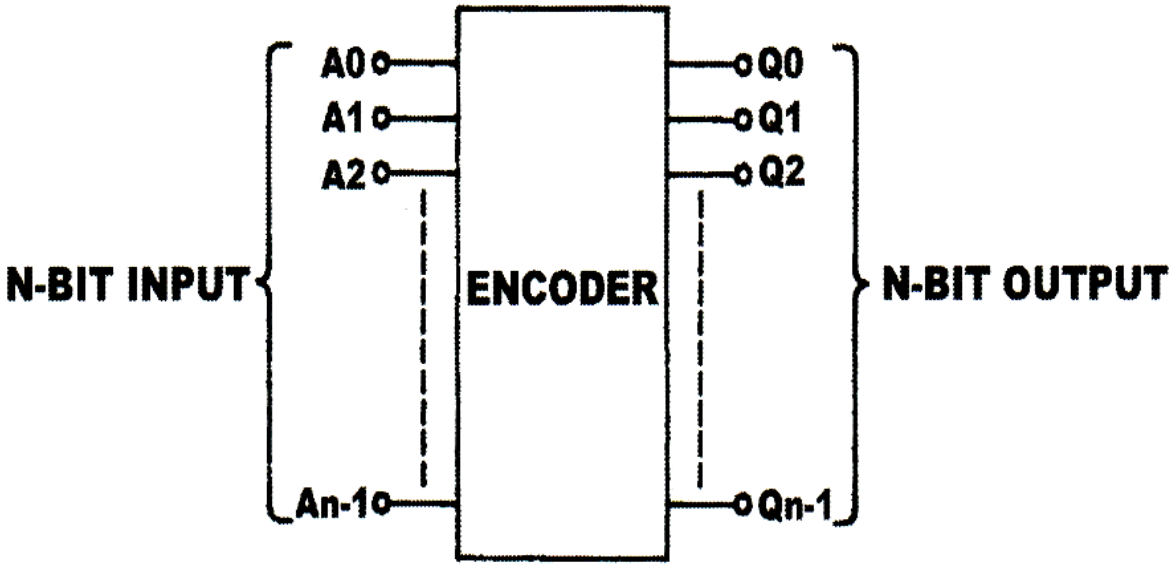


Fig. 2-61

Octal to Binary Encoder

An octal to binary encoder is shown in Fig. 2-62. There are 8 octal inputs A1~A7 (0~7); and three binary outputs Q0, Q1, Q2 (000 ~ 111). If input A0="0" the corresponding output Q2Q1Q0 is equal to "000".

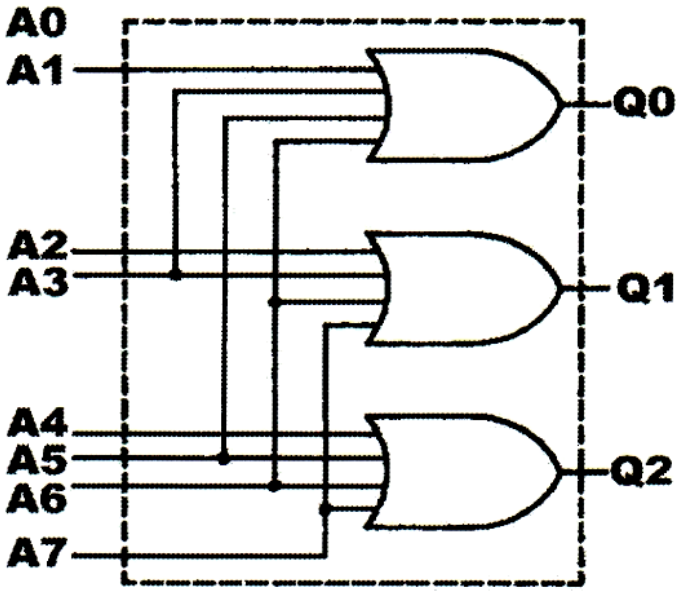


Fig. 2-62 Octal -Binary encoder

Actually, A0 is not connected to the gate input. If A1="1" then Q2Q1Q0=001. When A2="1" the output Q2Q1Q0=010. There can't be more than one "1" among the inputs. For example, if A2="1" and A3="1" simultaneously, Q2Q1Q0=011. If A3, A4 both are "1" at the same time, Q2Q1Q0=111. Both outputs are incorrect.

Matrix Encoder

If no commercially available encoders fits the require specification, one could be built by using diodes. Fig. 2-63 shows a simple matrix encoder build with diodes.

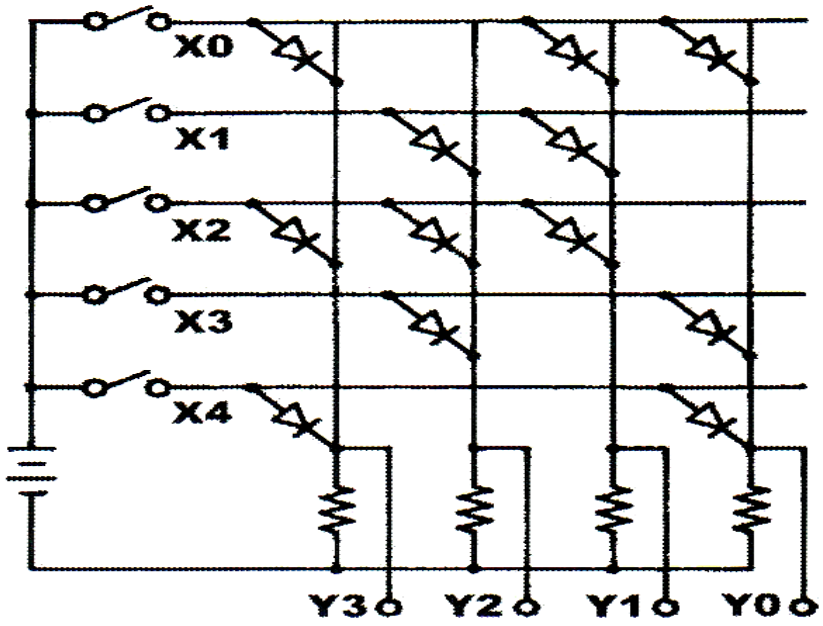


Fig. 2-63 Matrix encoder

Only one of X0~X4 will be triggered at a time. When X0="1", Y3Y2Y1Y0="1011"
When X1="1 ", Y3Y2Y1 Y0="0110".

In digital circuits sometimes it is critical to process various input signals in order of priority. One particular type of encoder called "Priority Encoder", which process inputs in order of priority should be used in such circuits. When an input gate with higher priority is triggered, the output will correspond to this high priority input regardless of the states of lower priority inputs are in. The 74147 is a 9-1 priority BCD output encoder, the input priority runs in ascending order, gate 1 has the lowest and gate 9 has the highest priority. The outputs are in BCD codes. Table 2-27 is the truth table for the 74147 10-to-4 priority encoder.

INPUT									OUTPUT			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Table 2-27 74147 Truth Table

The 74147 is triggered by the low logic state. When inputs 1 ~ 9 are all in high state, output DCBA="HHHH". When input 2 and 5 are triggered simultaneously the output is determined by input 5, which has higher priority than input 2. When inputs 2, 5 and 7 are triggered together, input 7 will determine the output.

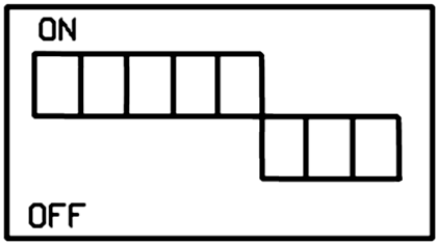
EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; Modules DLLT-EM05: Assembled Logic Circuits (4) Experiment

EXERCISE

Constructing a 4-to-2 Encoder with Basic Gates

1. Make sure the Fault Simulator DIP Switch follows the below setting:



2. Insert connection clips according to Fig. 2-64.

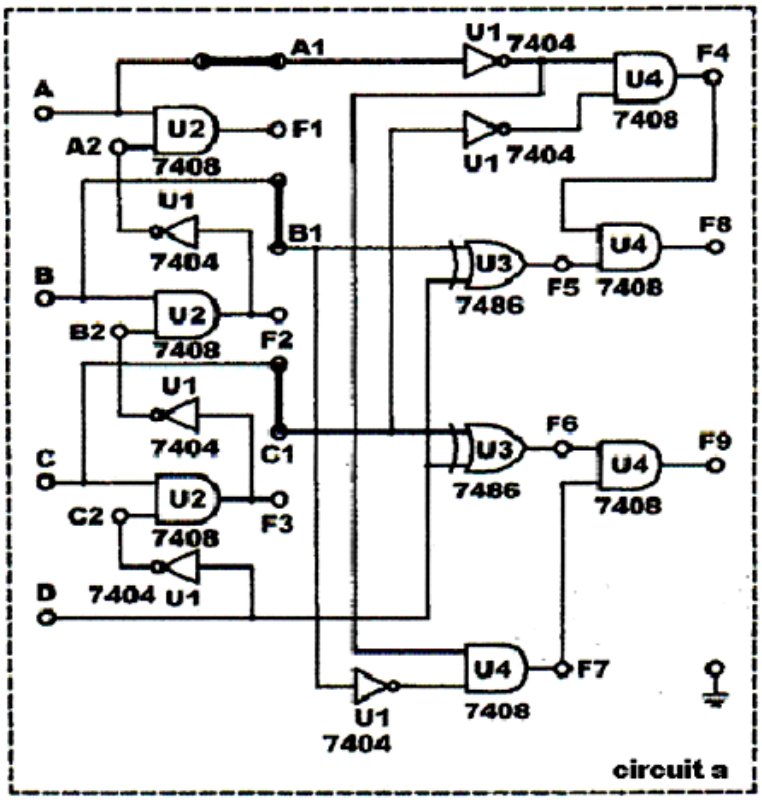


Fig 2-64

3. Connect Vcc to +5V.

4. Connect inputs A-D to Data Switches SW0 ~ SW3 respectively; outputs F8 and F9 to Logic Indicator L0 and L1.

5. Follow the input sequences for D, C, B, A in Table 2-28 and record the output states.

D	C	B	A	F8	F9
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

Table 2-28

6. Remove the connection clip between A and A1; insert it between A1 and F1 as shown in Fig. 2-65. All other connections remain the same. Follow the input sequences in Table 2-29 and record output states.

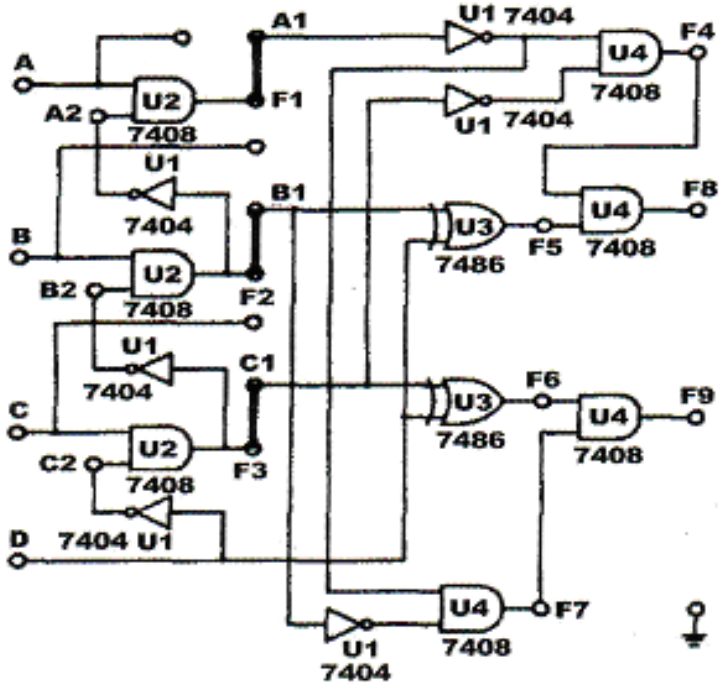


Fig. 2-65

D	C	B	A	F8	F9
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

Table 2-29

7. Compare the outputs states in Table 2-28 and 2-29. What is the difference between them?

RESULTS

1. Encoders have more input gates than output gates.

2. Output codes of encoders can only be read by professionals.

3. The output of encoders should be decoded by decoders.

FAULT SIMULATIONS

1. Use the circuit of Module DLLT-EM05 circuit a as an encoder without priority. Determine its truth tables under these conditions:
    1. S1 is open
    2. S2 is open
    3. S3 is open

5-2 Decoder Circuit

OBJECTIVE

Understand the operating principles of decoder circuits.

DISCUSSION

A decoder is a logic circuit that will detect the presence of a specific binary number or word. The input to the decoder is a parallel binary number and the output is a binary signal that indicates the presence or absence of that specific number.

The AND gate can be used as a basic decoder circuit, since the AND gates's output will be a binary 1 only when all inputs are binary 1. Proper connections of AND gate's inputs to the data will ensure detection of any binary number.

Binary-to-Octal Decoder
A binary-to-octal decoder is shown in Fig. 2-67. There are 3 binary inputs A, B, C and 8 octal outputs Q0~Q7. If CBA= "010" output Q2= "1". When CBA= "111" output Q7= "1".

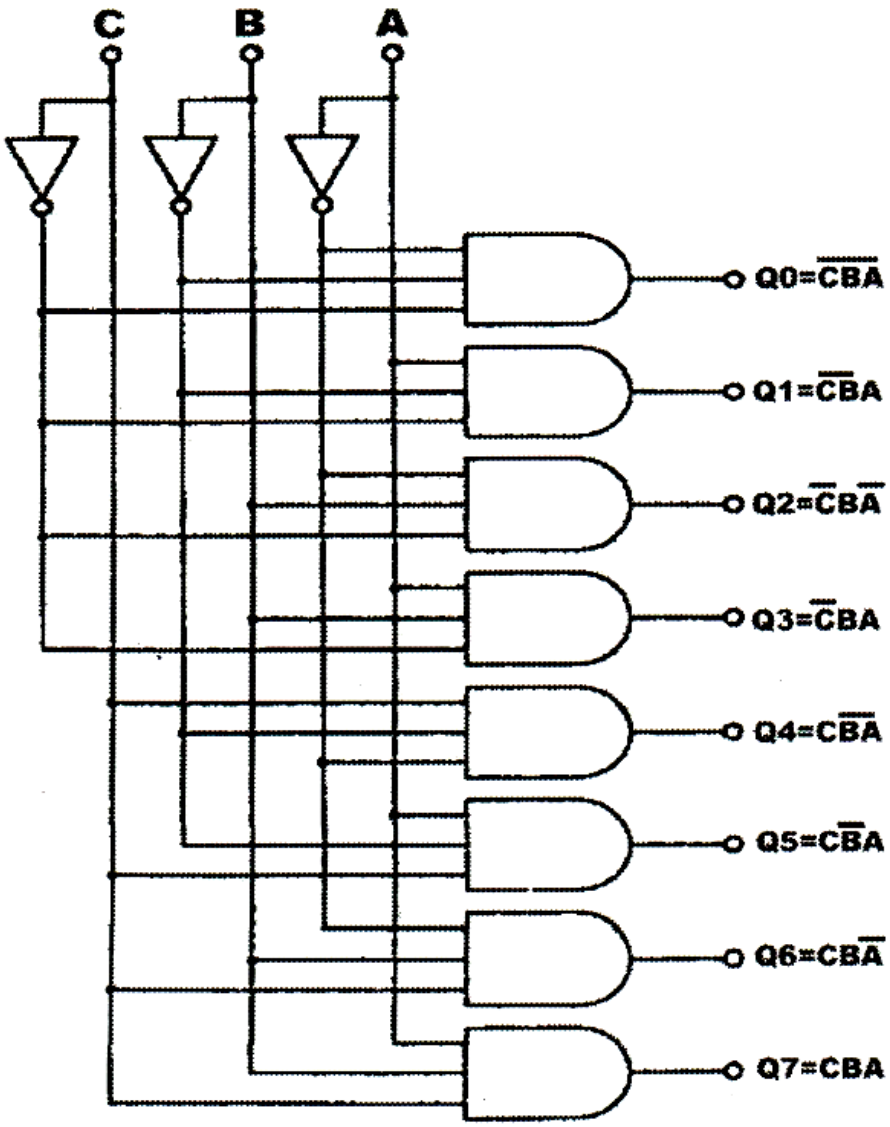


Fig. 2-67

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; DLLT-EM05: Assembled Logic Circuits (4) Experiment Module; Multimeter

EXERCISE

(a) Constructing a 2-to-4 Decoder with Basic Gates

1. Circuit c of module DLLT-EM05 will be used in this section of the experiment. Connect Vcc to +5V.

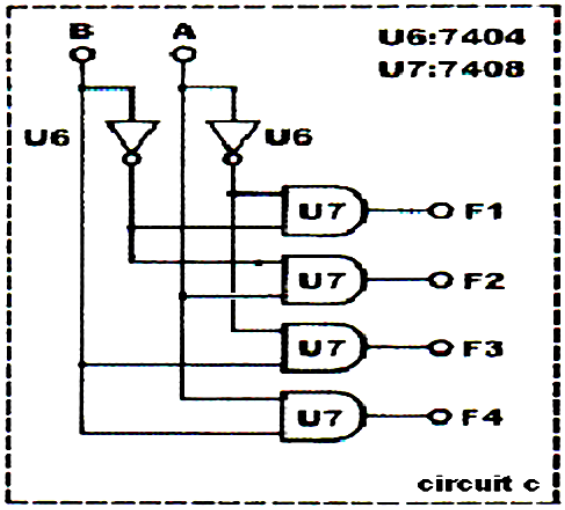


Fig. 2-68

2. Connect inputs A, B to Data Switches SW0 and SW1. Connect outputs F1-F4 to Logic Indicators L0 ~ L3 respectively.

3. Follow the input sequences for A and B in Table 2-31 and record output states.

B	A	F1	F2	F3	F4
0	0				
0	1				
1	0				
1	1				

Table 2-31

(b) BCD-to-7-Segment Decoder

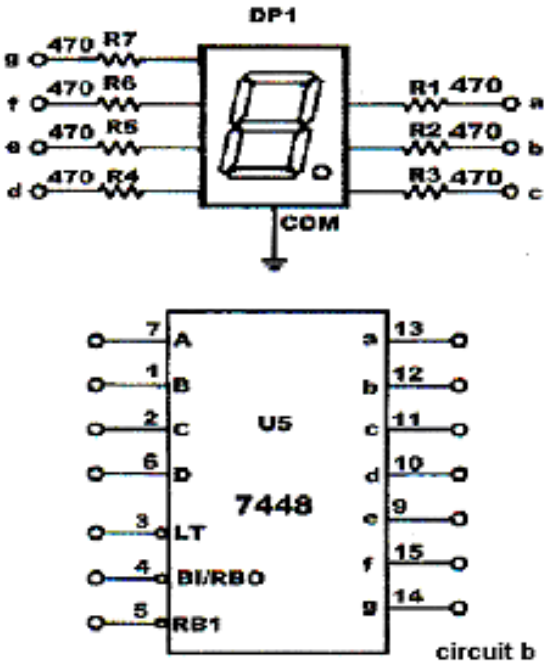


Fig. 2-70

1. Connect inputs A, B, C, D of U5 (7448) on circuit b of module DLLT-EM05 to Data Switches SW3, SW2, SW1, and SW0 respectively. The 7448 is a BCD-to-7-segment decoder/driver with internal pull-up outputs. Connect "RBI" to DIP Switch 1.0; "BI/RBO" to L0; "LT" to DIP1.1. Set DIP 1.0 and 1.1 to "HIGH".

2. Follow the input sequences for D, C, B, A in Table 2-33 and record outputs of the 7-segment display.

3. Set DIP1.1 to "LOW" while DIP1.0 remains "HIGH". Repeat step 2. Are the outputs any different from step 2?

D	C	B	A	Display
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Table 2-33

4. Set DIP1.0 to "LOW" and DIP1.1 to "HIGH". Repeat step 2. Compare outputs with step 2 between DCBA=0000-1001. Are the outputs different?

RESULTS

1. Decoder has the exact opposite functions of the encoder.

2. Two of the most direct applications of decoders are with numbers and words.

3. The 7442 is a 3 line-to-8 line decoder if D=0.

FAULT SIMULATIONS

1. Two separate input/output sequences for the decoder circuit of Fig. 2-68 are given below. Determine the fault(s) in each case.

B	A	F4	F3	F2	F1
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	0	0	0	0

B	A	F4	F3	F2	F1
0	0	0	1	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

3. Determine the fault(s) if U8 is used as decoder and the outputs are incorrect.

4. The outputs of BCD-to-7-segment decoder are incorrect. Try to determine possible causes.

DLLT-EM06 COMBINATIONAL LOGIC CIRCUITS

6-1 Encoder Circuit
- a. Constructing a 10-to-4 Encoder with TTL IC

6-2 Multiplexer Circuit
- a. Constructing a 2-to-1 Multiplexer
- b. Using Multiplexers to Create Functions.
- C. Constructing a 8-to-1 Multiplexer Circuit with TTL IC

6-3 Demultiplexer Circuit
- a Constructing a 2-output Demultiplexer with Basic Logic Gates
- b Constructing a 8-output Demultiplexer with CMOS IC

6-4 Digitally Controlled Analog Multiplexer / Demultiplexer Circuit
- a Analog Switch Characteristics
- b Bidirectional Transmission with CMOS IC Analog Switch

COMBINATIONAL LOGIC CIRCUITS EXPERIMENTS

Combinational logic circuits are constructed with basic logic gates. Its output will correspond only to the current input, previous inputs and outputs can't influence the current output. Therefore the output of any combinational logic circuits can be expressed by Boolean functions.

The major component of a combinational logic circuit includes Input Variables; Logic Gates and Output Variables. The input variable could be either higher or lower than the output variable but both are binary signals, or "0" and "1".

Assuming there are "n" input variables, there will be 2 possible input combinations, each with one corresponding output combination. Before designing and constructing a combinational logic circuit the following information should be taken into consideration:

1. Truth tables of logic gates
2. Boolean Function
3. Karnaugh Map
4. de Morgan's Theorem

The following combinational logic gates are used very often and they are discussed in this chapter, along with many other combinational logic gates.

1. Combinational logic circuits with NAND and NOR gates
2. AND-OR-INVERTER (A-O-I) gate
3. XOR gate
4. Open-collector gates
5. Tristate gate
6. Arithmetic circuits
7. Encoder and decoder circuits
8. Multiplexer and demultiplexer circuits
9. Comparator circuits

6-1 Encoder Circuit

OBJECTIVE

Understand the operating principles of encoder circuits.

DISCUSSION

An encoder is a combinational logic gates that accept one or multiple inputs and generates a specific output code. Only one input is triggered at a time. An encoder with n-bit inputs and n-bit outputs is shown in Fig. 2-61. When one of the inputs is triggered there will be a n-bit output code at the outputs.

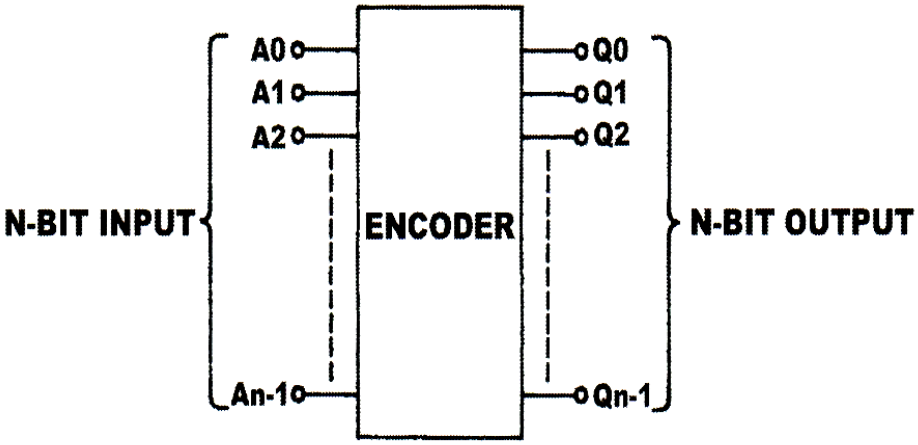


Fig. 2-61

Octal to Binary Encoder

An octal to binary encoder is shown in Fig. 2-62. There are 8 octal inputs A1~A7 (0~7); and three binary outputs Q0, Q1, Q2 (000 ~ 111). If input A0="0" the corresponding output Q2Q1Q0 is equal to "000".

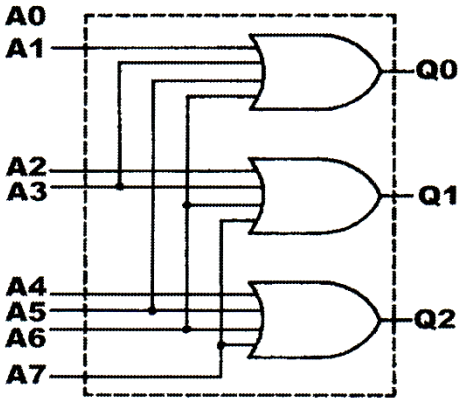


Fig. 2-62 Octal -Binary encoder

Actually, A0 is not connected to the gate input. If A1="1" then Q2Q1Q0=001. When A2="1" the output Q2Q1Q0=010. There can't be more than one "1" among the inputs. For example, if A2="1" and A3="1"

simultaneously, Q2Q1Q0=011. If A3, A4 both are "1" at the same time, Q2Q1Q0=111. Both outputs are incorrect.

Matrix Encoder

If no commercially available encoders fits the require specification, one could be built by using diodes. Fig. 2-63 shows a simple matrix encoder build with diodes.

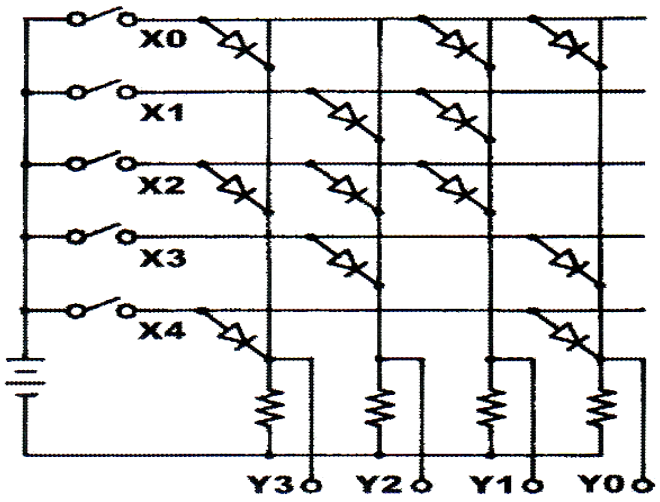


Fig. 2-63 Matrix encoder

Only one of X0~X4 will be triggered at a time. When X0="1", Y3Y2Y1Y0="1011"
When X1="1 ", Y3Y2Y1 Y0="0110".

In digital circuits sometimes it is critical to process various input signals in order of priority. One particular type of encoder called "Priority Encoder", which process inputs in order of priority should be used in such circuits. When an input gate with higher priority is triggered, the output will correspond to this high priority input regardless of the states of lower priority inputs are in. The 74147 is a 9-1 priority BCD output encoder, the input priority runs in ascending order, gate 1 has the lowest and gate 9 has the highest priority. The outputs are in BCD codes. Table 2-27 is the truth table for the 74147 10-to-4 priority encoder.

INPUT									OUTPUT			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Table 2-27 74147 truth table

The 74147 is triggered by the low logic state. When inputs 1 ~ 9 are all in high state, output DCBA="HHHH". When input 2 and 5 are triggered simultaneously the output is determined by input 5, which has higher priority than input 2. When inputs 2, 5 and 7 are triggered together, input 7 will determine the output.

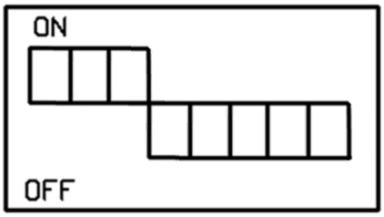
EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer; Module DLLT-EM06: Assembled Logic Circuits (5) Experiment

EXERCISE

Constructing a 10-to-4 Encoder with TTL IC

5. Make sure the Fault Simulator DIP Switch follows the below setting:



6. The 74147 (U7) on circuit a of module DLLT-EM06 is used in this section of the experiment. Connect Vcc to +5V.

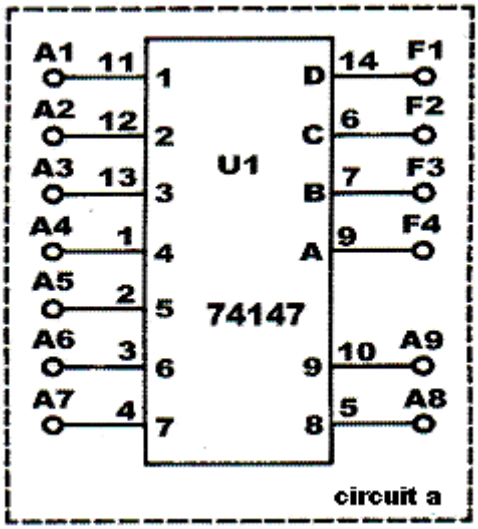


Fig. 2-66

7. Connect inputs A0 ~ A8 to DIP Switches 1.0 ~ 1.7, A9 to 2.0. Connect outputs F1 ~ F4 to Logic indicators L1 ~ L4. Follow the input sequences given in Table 2-30 and record output states.

A9	A8	A7	A6	A5	A4	A3	A2	A1	F4	F3	F2	F1
0	1	1	1	1	1	1	1	1				
0	0	1	1	1	1	1	1	1				
1	1	1	1	1	1	1	1	0				
1	1	1	1	1	1	1	0	0				
1	1	1	1	1	1	0	1	1				
1	1	1	1	1	0	0	0	0				
1	1	1	1	0	1	1	1	1				
1	1	1	1	0	0	0	1	1				
1	1	1	0	1	1	1	0	0				
1	1	0	1	1	0	1	1	0				
1	1	0	0	0	1	1	1	1				
1	0	0	0	0	0	1	1	1				

Table 2-30

RESULTS

4. Encoders have more input gates than output gates.

5. Output codes of encoders can only be read by professionals.

6. The output of encoders should be decoded by decoders.

FAULT SIMULATIONS

2. Use the circuit of Module DLLT-EM05 circuit a as an encoder without priority. Determine its truth tables under these conditions:
    1. S1 is open
    2. S2 is open
    3. S3 is open

6-2 Multiplexer Circuit

OBJECTIVE

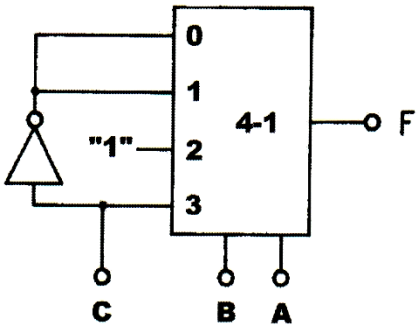
Understand the operating principles and construction of multiplexers.

DISCUSSION

Multiplexer, or MUX, is a logic circuit that select and route any number of inputs to a single output. One of the multiple inputs are selected by the selector gate and routed to the single output. The number of selector gates determines the capacity of a multiplexer. For example, if a certain MUX has only one selector gate, it is referred to as a "2 line-to-1 line MUX" because one selector can only select from two inputs.

A MUX with 3 selector gates is called "8 line-to-1 line MUX", since 3 selectors are capable of selecting an output from 8 inputs (2^3=8). MUX is also referred to as "Data Selector" because it selects one output from among many inputs.

Function expression, such as F (CBA) =Σ (0, 1, 2, 6, 7), can be easily executed on MUX. The function "F" generates the sum of products (CB+CB) from states 0, 1, 2, 6, 7. Refer to the 4 line-to-1 line MUX below, the output is determined by states of selectors A, Band C. When CBA=000, 001, 010, 110, 111 the output F is 1. In all other states F=0.



EQUIPMENTS REQUIRED

DLTT-1300 Digital Logic Lab Trainer, Module DLLT-EM06: Assembled Logic Circuits (5) Experiment

EXERCISE

a) Constructing a 2-to-1 Multiplexer

1. Circuit e of module DLLT-EM06 will be used as a 2-to-1 MUX.

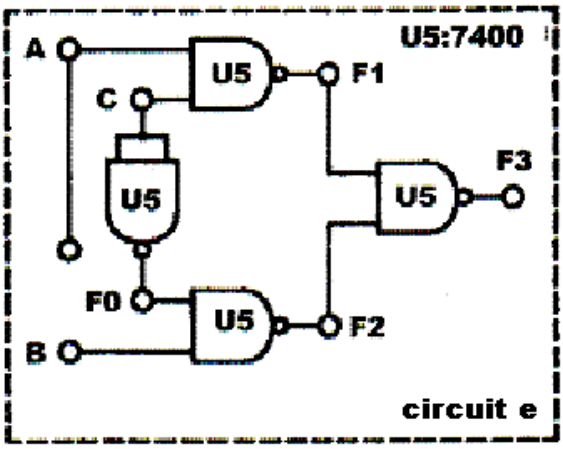


Fig. 2-71

2. Connect inputs A, B to Data Switches SW0, SW1; selector C to SW2.
   Connect output F3 to Logic Indicator L0.

3. Follow the input sequences in Table 2-34 and record states of F3. Which input (A or B) determines the output?

C	B	A	F3
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 2-34

(b) Using Multiplexers to Create Functions

1. Circuit f of module DLLT-EM06 will be used in this section of the experiment to create functions.

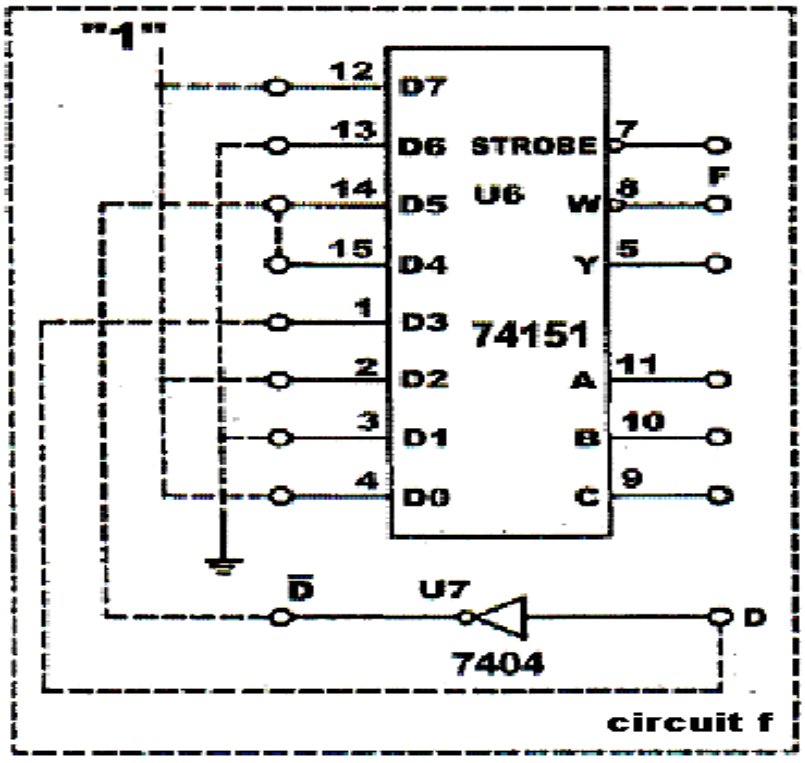
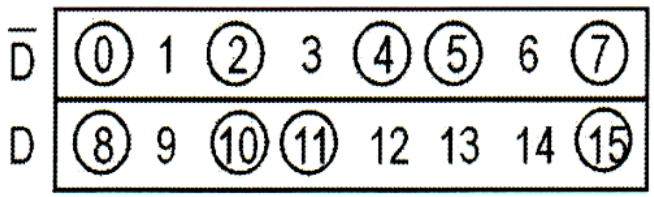


Fig. 2-72 shown circuit f of DLLT-EM06

2. Use U6 (74151) to create this function:
   F (D, C, B, A) = $\sum$(0,2,4,5,7,8,10,11,15)



Place connection leads according to Fig. 2-72 to complete the function shown above. Since D, C, B, A has 16 possible variations and the 74151 has only 8 variations, D will be used as the data input.

3. Connect inputs D, C, B, A to Data Switches SW3, SW2, SW1, SW0 respectively. Connect output Y to Logic Indicator L0. Follow the input sequences below and record output states.

D	C	B	A	Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

(c) Constructing a 8 to 1 Multiplexer Circuit with TTL IC

1. U6 (74151) on circuit f of module DLLT-EM06 will be used in section of the experiment.

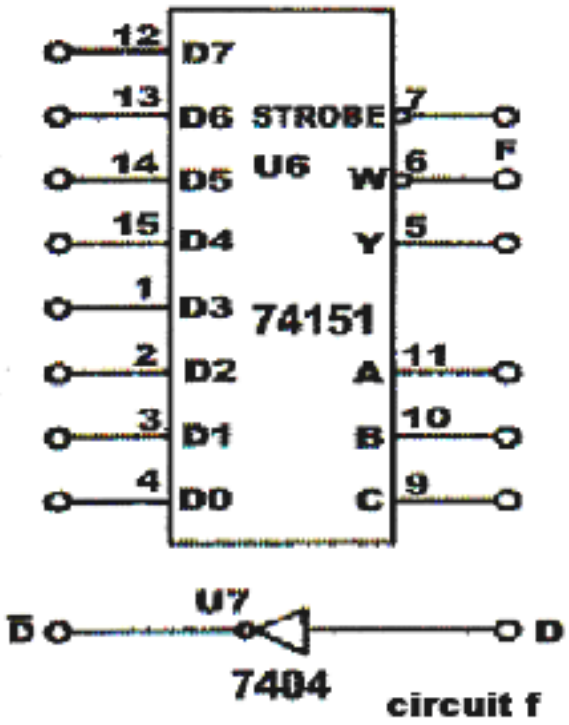


Fig. 2-73

6. Refer to the data book for specifications of the 74151.

   When CBA = "000", data at D0 is send to output F.
   When CBA = "010", data at D2 is send to output F.
   When CBA = "111 ", data at D7 is send to output F.
   The IC will function properly only when STROBE = "0".
   Y will remain "0" when STROBE ="'I".

7. Connect inputs D0 ~ D7 to DIP Switch 1.0 ~ 1.7; inputs C, B, A to DATA Switches SW2, SW1, SW0. Follow the input sequences in Table 2-35, adjust D0 ~ D7 and record output states. Determine on which input among D0 ~ D7 does F depend on.

C	B	A	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 2-35

RESULTS

1. MUX circuits has multiple inputs but only one input is selected at a time.

2. The execution of Boolean functions will be much simpler if standard MSI multiplexer devices are used. The need for SSI gates connection is also eliminated, reducing the number of ICs required as well as power consumption.

3. TTL multiplexer ICs includes: 7497, 74167, 74164, 74153, 74157, 74151, 74152, 74154.

FAULT SIMULATIONS

U5a, U5b, U5c on circuit e of module DLLT-EM06 are used as a MUX circuit. The data at B can't be selected when C="0" and the output F3 remains "0". What could cause this problem?

6-3 Demultiplexer Circuit

OBJECTIVE

Understand the operating principles and construction of demultiplexer circuits.

DISCUSSION

A demultiplexer, or DMUX, is basically a logic circuit that is exact opposite of a multiplexer. DMUX has a single input and multiple outputs. The input can be connected to any one of the many outputs through the selector terminal. The DMUX is also referred to as "Data Distributor" or "Data Router". Its pin assignment diagram is shown in Fig. 2-74 (a).

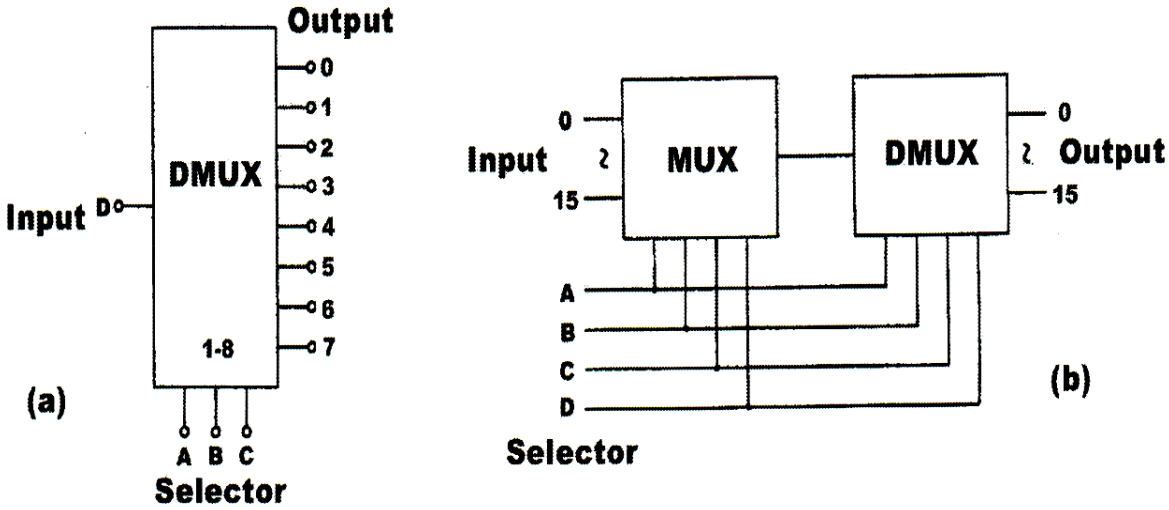


Fig. 2-74

When all three selector terminals A, B and C are in low logic state (CBA=000), data at input D is send to output number 0. When CBA=010, the input is send to output number 2. Collective state of selectors determines the location of output data. When CBA=111, data is send to the last output (output number 7). By

combining MUX and DMUX, long distance transmission systems can be set up, increasing the efficiency of transmission lines. Fig. 2-74 (b) shows a MUV-DMUX combinational circuit with 16 inputs, 16 outputs and 4 selectors.

EQUIPMENTS REQUIRED

DLLT-1300 Digital Logic Lab Trainer, DLLT-EM06: Assembled Logic Circuits (5) Experiment Module

EXERCISE

(a) Constructing a 2-output Demultiplexer with Basic Logic Gates

1. Insert connection clip according to Fig. 2-75. Connect A to Data Switch SW0; C to SW3; F1 and F2 to Logic Indicators L0 and L1 respectively.

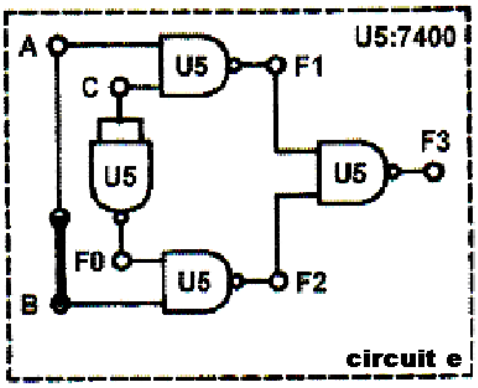


Fig. 2-75

2. Set C to "0" and change data at input A. Observe how F1 and F2 changes. Set C to "1 ", change A and observe how F1 and F2 react to changes of A.

(b) Constructing a 8-output Demultiplexer with CMOS IC

1. U2 (4051) on circuit e of module DLLT-EM06 is used in this section of the experiment.

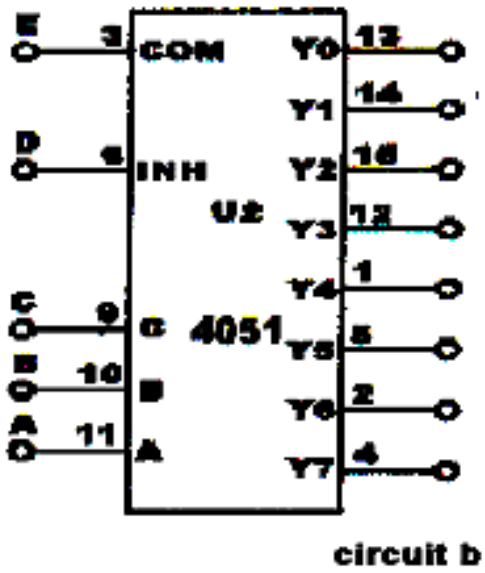


Fig. 2-76

2. Connect E to 1 Hz TTL Standard Frequency; D to DIP1.1; A to SW0; B to SW1; C to SW2; outputs Y0 ~ Y7 to Logic Indicators L0 ~ L7 respectively.

3. At D=0, observe outputs Y0 ~ Y7. Did the outputs change as the input sequence is applied?

   At D=1, observe outputs Y0 ~ Y7. Did the outputs change as the input sequence is applied?

   Which state of D changes the outputs?

   Using the same sequence for E (1-0-1-0), follow the sequence for A, B and C given in Fig. 2-36 (a). Record output states.

C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0								
0	0	1								
0	1	0								
0	1	1								
1	0	0								
1	0	1								
1	1	0								
1	1	1								

Table 2-36 (a)

4. Reconstruct the circuit by removing the connections done in step 2. Connect Y0 ~ Y7 to DIP1.0 ~ 1.7; E to L0; D to SW3; C to SW2; B to SW1; A to SW0.

   Change the state of Y0 ~ Y7 from 1 to 0 to 1 (1-0-1) and observe E. Did E follow changes to Y0 ~ Y7?

Follow the input sequence for C, B, A in Table 2-36 (b) and observe the relationship between E and Y0 ~ Y7. Is Table 2-36 (b) correct?

C	B	A	E
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2
0	1	1	Y3
1	0	0	Y4
1	0	1	Y5
1	1	0	Y6
1	1	1	Y7

Table 2-36 (b)

Does the relationship between E and Y0-Y7 in Table 2-36 (b) still apply when D changes state?

RESULTS

1. Depending on the selector terminals (decoders), MUX and DMUX will either select or distribute input data.

2. 74155 and 174154 are two TTL demultiplexer ICs.

FAULT SIMULATION

If the output of U2 (4051) on module DLLT-EM06 block b does not match the state of the selector terminals, what could the problem(s)?

6-4 Digitally Controlled Analog Multiplexer /Demultiplexer Circuit

OBJECTIVE

Understand the characteristics of analog multiplexer and demultiplexer.

DISCUSSION

Multiplexers and demultiplexers made from TTL gates can only transmit data in one direction but those made with CMOS gates can transmit data bidirectional. In other words, the inputs and outputs of CMOS multiplexer/demultiplexer circuits are interchangeable.

The characteristics of CMOS gates, such as CD4066, allow it to be used as analog switches. The symbol and equivalent circuit of a CMOS analog switch are shown in Fig. 2-78 (a); (b) respectively.

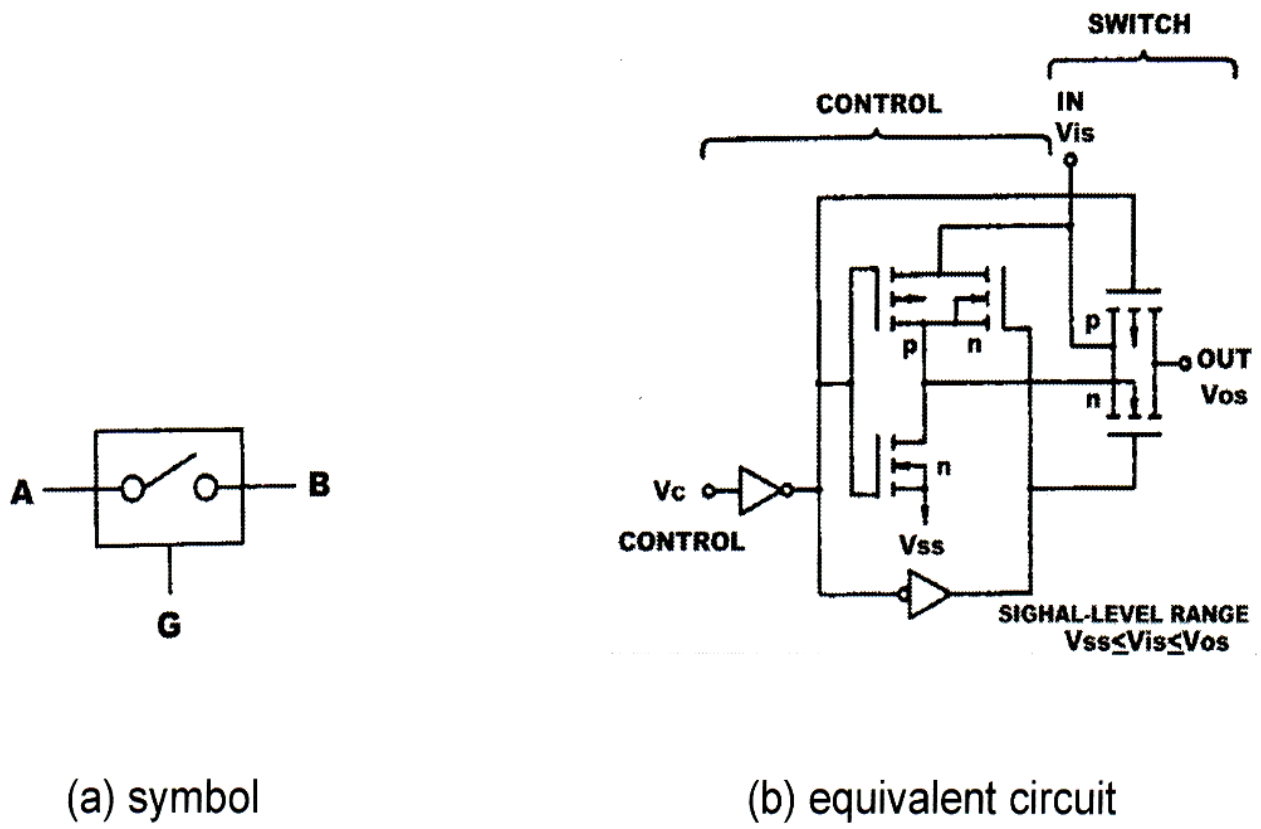


Fig. 2-78 CMOS analog switch circuit

From Fig. 2-78 (a), we can see that there is a switch between A and B. This switch enables bidirectional data transmission by allowing both A and B to be used as input when the other side is the output. Fig. 2-79 shows a typical CMOS IC which is capable of analog/digital bidirectional data transmission.

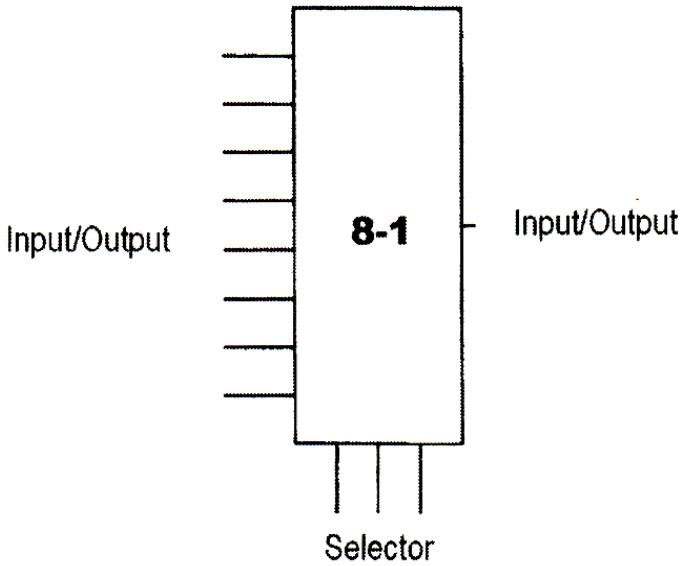


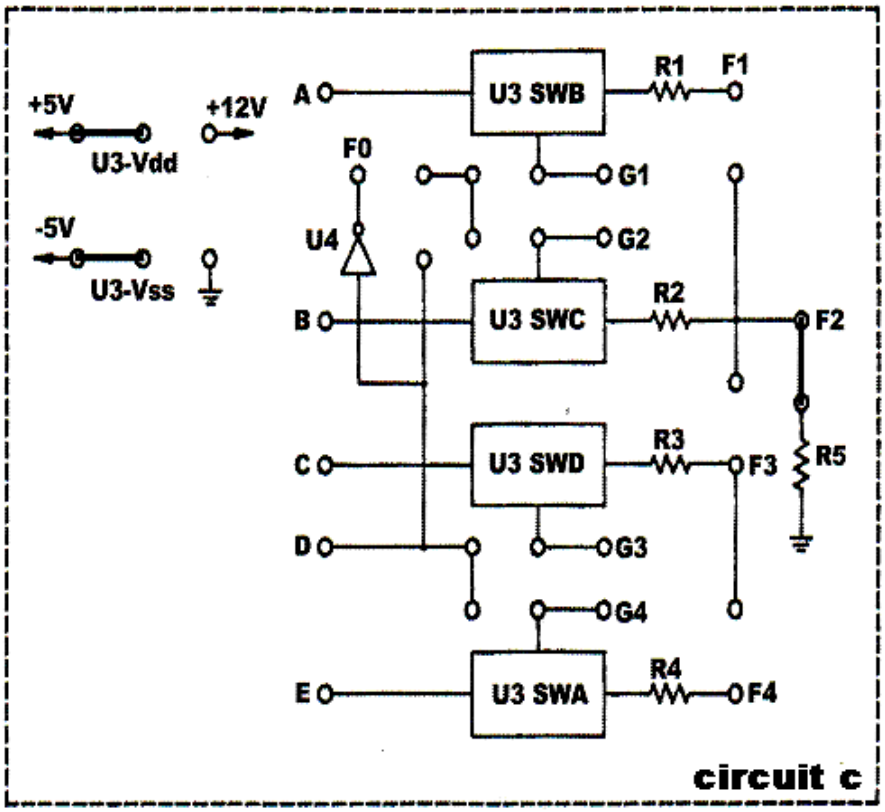
Fig. 2-79

EQUIPMENTS REQUIRED

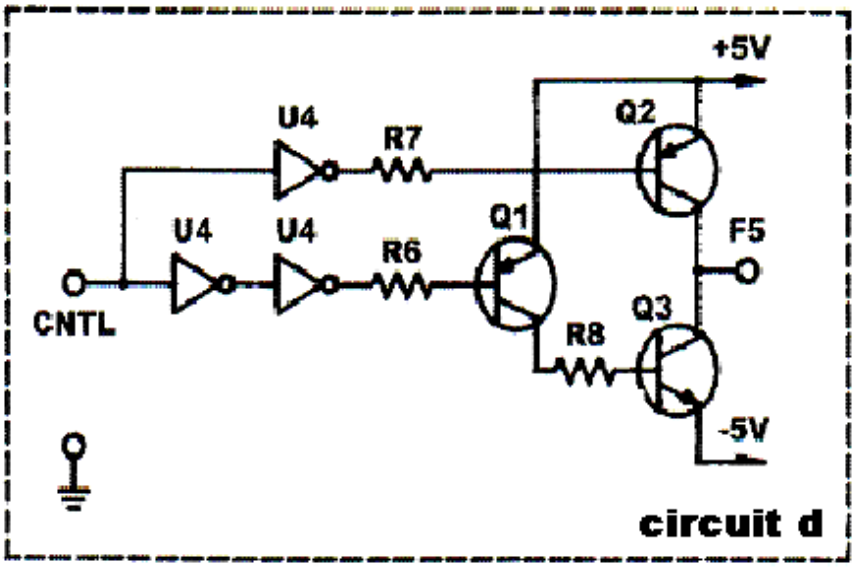
DLLT-1300 Digital Logic Lab Trainer; Module DLLT-EM06; Oscilloscope; Function Generator; Multimeter

EXERCISE

(a) Analog Switch Characteristics



(a)



(b)

Fig. 2-80

1. Insert a connection clip between R2 and R5 on circuit c of module DLLT-EM06 to complete the circuit of Fig. 2-81.

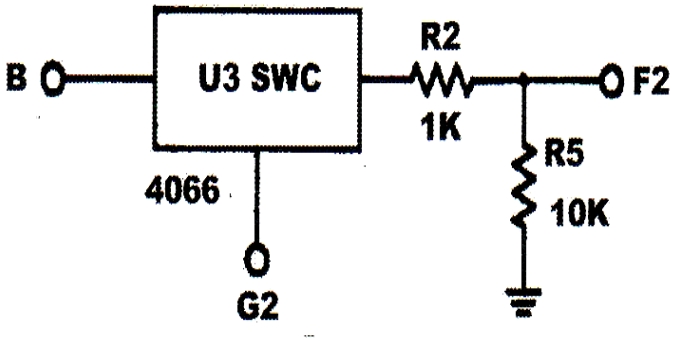


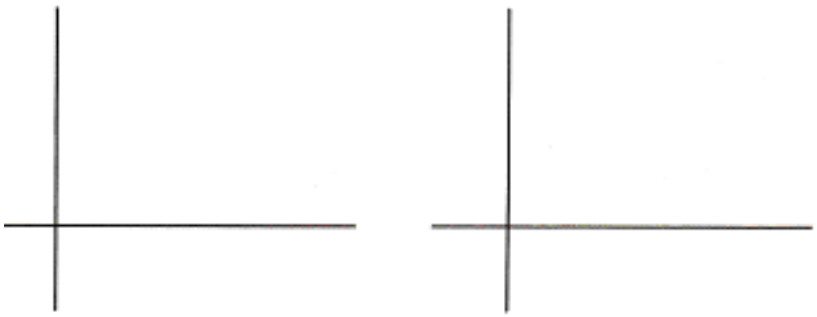
Fig. 2-81

2. Connect Vdd and Vss on circuit c of module DLLT-EM06 to +5V and -5V respectively [Fig. 2-80 (a)]. Connect input A to Data Switch SW0, and output F5 to the selector input G2 of Fig. 2-80 (b) [Module DLLT-EM06 circuit d].

   F5=+5V when SW0="1 "; F5=-5V when SW0="0".

3. Connect B to the 60Hz 5Vp-p sine wave output of a Function Generator.

4. Measure and record voltage and waveform at B (VB) and F2 (VF2) below.



5. Measure and record VB, VF2 at SW0="0" (SW0="OFF"). Calculate the switch resistance (Rg) by using this equation:

$$VF2 = \frac{10K\Omega \times VB}{(Rg + 1K\Omega) + 10K\Omega}$$

   VB = _____; VF2 = _____; Rg = _____ = Roff

6. Measure and record VB, VF2 at SW0="1 ", F5=+5V, G2=+5V. Calculate Rg under this condition with the same equation.

V= _____; VF2= _____; Rg= _____ =Ron

7. Compare Ron with Roff. Which is larger? What is the ratio?
   $\frac{Roff}{Ron}$ =_____; express the ratio in dB (dB = log $\frac{Roff}{Ron}$)

   Compare the calculated ratio with the theoretical ratio of the 4066 in the data book. What is the difference?

   Actual Ratio = _____
   Theoretical Ratio = _____
   Difference = _____

8. Switch the input and output (Use B as the output and F2 as the output). Connect F2 to the 60Hz, 5p-p sine wave output of the Function Generator. Connect output B to R5, measure and record output voltages (Vo) under these two conditions:

   G2 = -5V, Vo = Vo- = _____
   G2 = +5V, Vo = Vo+ = _____

   Calculate the ratio of Vo-/Vo+. Is it close to the ratio of Roff/ Ron?

9. Connect Vss to GND and G2 to SW0.

   A. Connect B to 5Vp-p, 60 Hz sine wave.

   (1) when G2 = GND, Vo = _____
   (2) when G2 = +5V, Vo = _____

   B. Connect B to 5Vp-p, 1 KHz sine wave.

   (1) when G2 = GND, Vo = _____
   (2) when G2 = +5V, Vo = _____

10. Insert connection clips on circuit c of module DLLT-EM06 to complete the circuit of Fig. 2-82. Connect Vdd to +12V and Vss to GND.

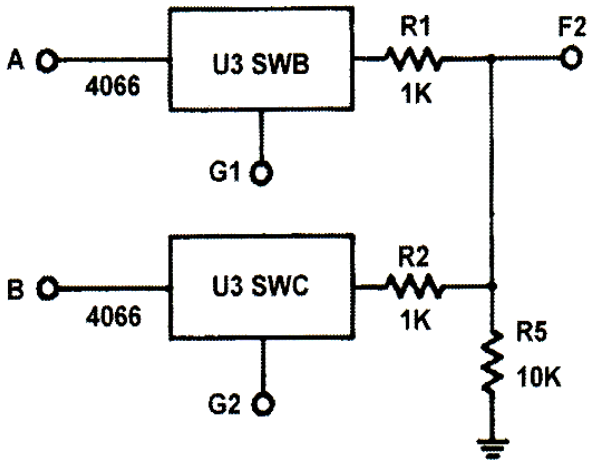
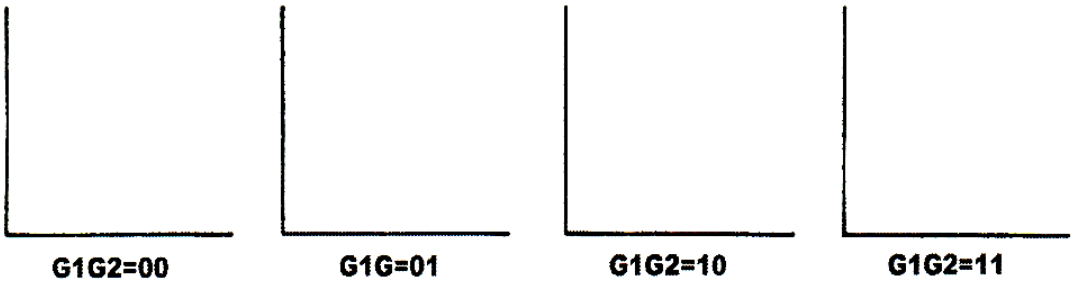


Fig. 2-82

11. Connect G1 to SW0; G2 to SW1; A to 60Hz, 5Vp-p sine wave and B to 1 KHz 5Vp-p sine wave. Measure and record output voltage Vo under the following conditions:



A. G1G2 = "00" B. G1G2 = "01" C. G1G2 = "10" D. G1G2 = "11"

(b) Bidirectional Transmission with CMOS IC Analog Switch

1. Construct the circuit of Fig. 2-83 on circuit c of module DLLT-EM06. Connect Vdd to +5V and Vss to -5V.

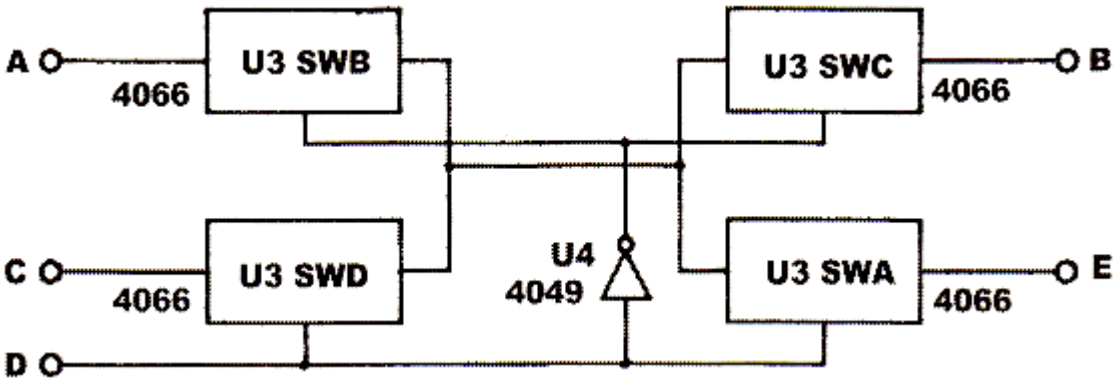
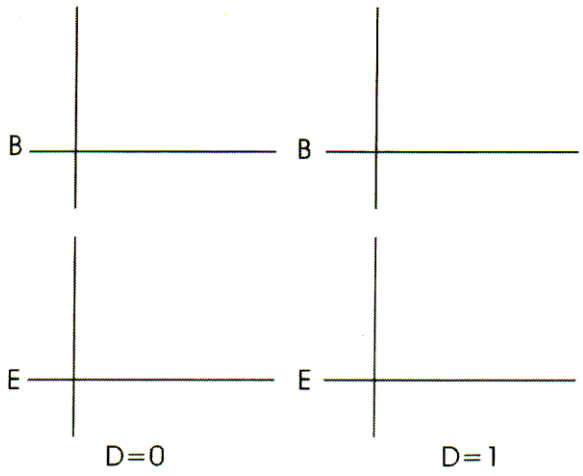


Fig. 2-83

2. Connect input A to the 60 Hz sine wave (TTL level) output of the Function Generator. Connect input C to the 1 KHz sine wave output (TTL level) and D to SW0.

3. Connect output B to CH1 and E to CH2 of the oscilloscope.

4. Observe and record the output waveforms at D="0" and D="1".



RESULTS

1 When the analog switch is turned ON, the input signal can barely be seen at the output.

3. Analog multiplexers/ demultiplexers are non-directional.

4. Analog switches can be used for both analog and digital signals.

5. Analog switches can use single voltage or dual ± voltages.

FAULT SIMULATION

1. A can transmit to B but C can't transmit to E for the circuit of Fig. 2-83. What could be the problem(s)?

2. For the circuit of Fig. 2-83, A and B are connected regardless of the status of the selector but there seemed to be some interference when C and E are connected. What could be the problem(s)?

3. What could be the problem when phase of D is reversed by U4 and the circuit does not function properly?

4. D is connected to F5 (±5V) on circuit d of module DLLT-EM06 but +5V can't be generated at F5. What could be the problem?